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Methods of Measurement for Semiconductor Materials, Process Control, and Devices

Quarterly Report

October 1 to December 31, 1971

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[1] Headquarters and Laboratories at Gaithersburg, Maryland, unless otherwise noted; mailing address Washington, D.C. 20234.
[2] Part of the Center for Radiation Research.
[3] Located at Boulder, Colorado 80302.

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Methods of Measurement for Semiconductor Materials, Process Control, and Devices

Quarterly Report, October 1 to December 31, 1971

W. Murray Bullis, Editor

Electronic Technology Division
Institute for Applied Technology
U.S. National Bureau of Standards
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For sale by the Superintendent of Documents, U.S. Government Printing Office, Washington, D.C. 20402
(Order by SD Catalog No. C13.46:727). Price 70 cents.

Frontispiece — Scanning electron microscope photomicrograph (magnification ~920 X) of an aluminum-aluminum ultrasonic wire bond after 76,000 power cycles. The bond was made with large loop height to reduce the flexure fatigue of the aluminum wire during power cycling. The pronounced hillock growth on the aluminum metallization also results from the power cycling. (See section 4.2)

FOREWORD

The Joint Program on Methods of Measurement for Semiconductor Materials, Process Control, and Devices was undertaken in 1968 to focus NBS efforts to enhance the performance, interchangeability, and reliability of discrete semiconductor devices and integrated circuits through improvements in methods of measurement for use in specifying materials and devices and in control of device fabrication processes. These improvements are intended to lead to a set of measurement methods which have been carefully evaluated for technical adequacy, which are acceptable to both users and suppliers, which can provide a common basis for the purchase specifications of government agencies, and which will lead to greater economy in government procurement. In addition, such methods will provide a basis for controlled improvements in essential device characteristics, such as uniformity of response to radiation effects.

The Program is supported by the National Bureau of Standards,* the Defense Nuclear Agency,† the U.S. Navy Strategic Systems Project Office,§ the U.S. Navy Electronics Systems Command,+ the Air Force Weapons Laboratory,¶ the Air Force Cambridge Research Laboratories,# the Advanced Research Projects Agency,× the Atomic Energy Commission,** and the National Aeronautics and Space Administration.†† Although there is not a one-to-one correspondence between the tasks described in this report and the cost centers through which the Program is supported, the concern of certain sponsors with specific parts of the program is reflected in planning and conduct of the work.

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† Through Order EA072-810. (NBS Cost Center 4259522).

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× ARPA Order 1889 Monitored by Space and Missile Systems Organization under MIPR FY76167100331. (NBS Cost Center 4254422).

** Division of Biology and Medicine. (NBS Cost Center 4254425).

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TABLE OF CONTENTS

PAGE

1. Introduction 2

2. Highlights 3

3. Semiconductor Materials

3.1. Resistivity 7

3.2. Gold-Doped Silicon 11

3.3. Infrared Methods 16

3.4. References 20

4. Semiconductor Process Control

4.1. Die Attachment Evaluation 22

4.2. Wire Bond Evaluation 29

4.3. References 44

5. Semiconductor Devices

5.1. Thermal Properties of Devices 46

5.2. Microwave Device Measurements 51

5.3. Carrier Transport in Junction Devices 53

5.4. Silicon Nuclear Radiation Detectors 61

5.5. References 64

Appendix A. Joint Program Staff 65

Appendix B. Committee Activities 66

Appendix C. Solid-State Technology & Fabrication Services 68

Appendix D. Joint Program Publications 69

LIST OF FIGURES

PAGE

1. Resistivity as a function of gold concentration in p-type silicon with initial resistivity ρ_i of 11, 20, and 93 Ω·cm 13
2. Infrared response spectra of two germanium gamma-ray detectors 18
3. Infrared response spectra of a commercial lithium-drifted silicon detector obtained before and after irradiation with fast neutrons 18
4. Infrared response spectra of three commercial lithium-drifted silicon detectors 18
5. Diode with controlled void 26
6. Models for heat flow patterns 28
7. Thermal response measurement system 28
8. SEM photomicrographs of ultrasonic aluminum wire bonds made with large loop heights showing variation in bond deformation 30
9. Device for polishing convex surfaces and grooves on bonding tools 32
10. SEM photomicrographs of ribbon wire bonds made with low power and long time 32
11. SEM photomicrographs of ribbon wire bonds made with normal power and time 32
12. SEM photomicrograph of lift-off pattern of carefully removed adherent second bond make with the same low-power, long-time bonding cycle used for the bonds in figure 10 showing the uniform nature of the welding 34
13. SEM photomicrograph of three bonds made with aluminum ribbon wire with cross-sectional dimensions 0.0005 by 0.0015 in. (13 by 38 μm) on a bonding pad 0.005-in. (127-μm) square 34
14. Simplified diagram of the pulse delay and phasing system used to monitor and study ultrasonic bonding 36
15. Bond formation pattern of a typical adherent bond 36
16. Oscilloscope displays of phased burst bonding cycle 37
17. Measured pull strength of single-level bond pairs for different hook positions 40

LIST OF FIGURES

PAGE

18. Measured pull strength of underformed, moderately deformed, and excessively deformed single-level first bonds for different hook positions 40

19. Measured pull strength of moderately deformed and excessively deformed single-level second bonds for different hook positions 40

20. Measured pull strength of single-level bond pairs as a function of the angle of pull in the plane of the bond loop 42

21. Pull configurations for two-level bonds 42

22. Difference between the value of the base-emitter voltage extrapolated to zero power and the d-c calibration value for a triple-diffused silicon power transistor 48

23. Common emitter current gain as a function of collector emitter voltage for a single-diffused, wide-base silicon power transistor 48

24. Vector diagram showing input-signal, transistor transfer function, extraneous error signal and output signal for a phase-delay measurement system 54

25. Maximum phase delay error due to extraneous coupling as a function of measurement frequency and isolation ratio 54

26. Photomicrograph of typical R-C plug-in network assembled on a TO-5 header 54

27. Delay time of a 2N2219 transistor measured on two systems of different types at frequencies from 3 to 30 MHz 58

28. Delay time of two high-frequency transistors each measured on two different systems of the same type 58

29. Transit time of a 2N2219 transistor derived from S-parameter measurements 60

30. Vector-voltmeter delay-time measuring circuit 60

LIST OF TABLES

PAGE

1. Capture Cross Sections for Electrons and Holes in *n*-Type and *p*-Type Gold-Doped Silicon 15
2. Measured and Calculated Minority Carrier Lifetimes in *p*-Type Gold-Doped Silicon 15
3. Comparison of Results of Junction-To-Case Temperature Difference Measurements for Devices with 20 Percent Chip-Void Area 24
4. Measurements to Determine Reproducibility of the Die Attachment Evaluation Equipment 24
5. Summary of Results of Ambient Exposure Tests 63

METHODS OF MEASUREMENT FOR SEMICONDUCTOR MATERIALS, PROCESS CONTROL, AND DEVICES

QUARTERLY REPORT

OCTOBER 1 TO DECEMBER 31, 1971

This quarterly progress report, fourteenth of a series, describes NBS activities directed toward the development of methods of measurement for semiconductor materials, process control, and devices. Significant accomplishments during this reporting period include the determination of the reasons for substantial differences in measurements of transistor delay time, a device characteristic frequently used as a screen in radiation hardness assurance tests, as measured with different instruments or with the same instrument at different frequencies; identification of an energy level model for gold-doped silicon that yields a calculated dependence of resistivity on gold concentration that agrees very well with experimental measurements on *p*-type gold-doped silicon; and finding of evidence that it does not appear to be necessary for an ultrasonic bonding tool to grip the wire and move it across the substrate metallization to make the bond. Work is continuing on measurement of resistivity of semiconductor crystals; study of gold-doped silicon; development of the infrared response technique; evaluation of wire bonds and die attachment; measurement of thermal properties of semiconductor devices, delay time and related carrier transport properties in junction devices, and noise properties of microwave diodes; and characterization of silicon nuclear radiation detectors. Supplementary data concerning staff, standards committee activities, technical services, and publications are included as appendixes.

Key Words: Alpha-particle detectors; aluminum wire; base transit time; carrier lifetime; die attachment; electrical properties; epitaxial silicon; gamma-ray detectors; germanium; gold-doped silicon; infrared response; methods of measurement; microelectronics; microwave diodes; nuclear radiation detectors; probe techniques (a-c); resistivity; semiconductor devices; semiconductor materials; semiconductor process control; silicon; thermal resistance; thermographic measurements; ultrasonic bonding; wire bonds.

1. INTRODUCTION

This is the fourteenth quarterly report to the sponsors of the Joint Program on Methods of Measurement for Semiconductor Materials, Process Control, and Devices. It summarizes work on a wide variety of measurement methods that are being studied at the National Bureau of Standards. Since the Program is a continuing one, the results and conclusions reported here are subject to modification and refinement.

The work of the Program is divided into a number of tasks, each directed toward the study of a particular material or device property or measurement technique. This report is subdivided according to these tasks. Highlights of activity during the quarter are given in Section 2. Section 3 deals with tasks on methods of measurement for materials; Section 4, with those on methods of measurement for process control; and Section 5, with those on methods of measurement for devices. References for each section are listed in a separate subsection at the end of that section.

The report of each task includes the long-term objective, a narrative description of progress made during this reporting period, and a listing of plans for the immediate future. Additional information concerning the material reported may be obtained directly from individual staff members connected with the task as indicated throughout the report. The organization of the Joint Program staff and telephone numbers are listed in Appendix A.

An important part of the work that frequently goes beyond the task structure is participation in the activities of various technical standardizing committees. The list of personnel involved with this work given in Appendix B suggests the extent of this participation. Additional details of current standardization activities not associated with a particular task are given in Section 2.

Background material on the Program and individual tasks may be found in earlier reports in this series as listed in Appendix D. From time to time, publications are prepared that describe some aspect of the program in greater detail. Current publications of this type are also listed in Appendix D. Reprints or copies of such publications are usually available on request to the author.

2. HIGHLIGHTS

Significant accomplishments during this reporting period include the determination of the reasons for substantial differences in measurements of transistor delay time, a device characteristic frequently used as a screen in radiation hardness assurance tests, as measured with different instruments or with the same instrument at different frequencies; identification of an energy level model for gold-doped silicon that yields a calculated dependence of resistivity on gold concentration that agrees very well with experimental measurements on *p*-type gold-doped silicon; and finding of evidence that it does not appear to be necessary for an ultrasonic bonding tool to grip the wire and move it across the substrate metallization to make the bond. Highlights of these and other technical activities are presented in this section; details are given in subsequent sections of the report. This section concludes with a summary of standardization activities not associated with a specific task being carried out by program staff members.

Resistivity — A modified collaborative reference program has been developed in response to the request by ASTM Committee F-1 on Electronics for NBS to supply silicon resistivity standards. Work to compare resistivity of silicon wafers as measured by capacitance-voltage (C-V) and four-probe techniques shows that the doping density determined by the C-V method is 10 to 25 percent less than that derived from the four-probe measurement. Comparison of C-V data on diffused wafers with measurements made by another laboratory indicates that difficulties in determining the capacitance of the diode in the presence of stray capacitances may be a major source of discrepancy.

Gold-Doped Silicon — Additional possible causes of the decrease of resistivity with increasing gold concentration in heavily gold-doped, *p*-type silicon were investigated. It was found that additional shallow acceptors were not being introduced unintentionally into wafers during gold diffusion so that this cause was eliminated from further consideration. Calculations based on a model that includes a shallow acceptor center coupled with the gold centers yield a resistivity dependence on gold concentration that agrees very well with experimental measurements on *p*-type, gold-doped silicon. Additional preliminary measurements of carrier lifetime were made by the surface photovoltage method in several *p*-type silicon wafers lightly doped with gold. Although the values obtained were generally in the same range as lifetime value calculated from capture cross section data in the literature, differences between the measured and calculated values were observed. Possible causes of these differences are being investigated.

Infrared Methods — Some insight has been gained as to the mechanism of the infrared response (IRR) of germanium and silicon *p-i-n* diodes with wide *i*-regions. The effect appears to be that of the impurity photo-EMF observed in *p-n* diodes. The IRR

of a neutron-irradiated lithium-drifted germanium diode showed enhancement of certain features in the spectrum. The IRR of four commercial lithium-drifted silicon detectors has been measured. A variety of features was observed in the spectra of unirradiated specimens and neutron-, proton-, and electron-irradiated specimens; the observed features are being interpreted in terms of defect levels.

Die Attachment Evaluation — Experimental investigations were completed in the evaluation of the applicability of thermal response measurements to the detection of voids in diode die attachment. Previous measurements indicated that, for the diode structure being studied, the transient thermal response was approximately three times as sensitive to the presence of voids in the die attachment as the steady-state thermal response or thermal resistance. It was concluded that the transient thermal response technique demonstrated sufficient sensitivity in diode structures that investigation of its applicability to the detection of voids in die attachment of transistor structures should be initiated. The earlier work on diodes has also shown that sensitivity to void sizes of both 20 and 40 percent of the chip bonding area was nearly the same. A theoretical study of the heat flow pattern in diodes with voids was begun in an attempt to understand the similarity of response in diodes with void areas of these sizes. In a search for means for simplifying the measurement it was found that the temperature coefficient of the forward voltage drop was essentially constant for a given lot of devices so that it is not necessary to measure this quantity for each device in a lot.

Wire Bond Evaluation — Several devices that had been power cycled 76,000 times at the Marshall Space Flight Center were examined with a scanning electron microscope; it was observed that, even though there were no failures, bond deterioration was pronounced in cases where the bond deformation was greater than two wire diameters. In continuing work on ultrasonic bonding of aluminum ribbon wire it has been found that alteration of the bonding schedule from the normal short-time, high-power conditions to longer time, lower power conditions improves the cosmetic appearance, increases the bond strength, and eliminates the heel crack. Measurement techniques were improved for the in-process study of ultrasonic wire bonding. In addition, a new modification of the ultrasonic bonding schedule, termed phased-burst bonding, has been introduced. Use of this schedule appears to result in increased bond adherence. Preliminary information has been developed that provides insight into the mechanisms of ultrasonic bonding. One significant finding is that it does not appear to be necessary for the tool to grip the wire and move it across the substrate metallization to make the bond. Experimental and statistical analysis of significant factors in the wire bond pull test continued with investigations of the effect of the angle between pull force and the bond wire on the measured pull strength.

Thermal Properties of Devices — Investigation was continued of the measurement of thermal resistance to compare the use of the collector-base voltage as the temperature sensitive parameter with the use of the emitter-base voltage. It was established that to compare measured values of transistor thermal resistance it is imperative to use the same temperature sensitive parameter, delay time, and measuring current, but further work is needed to determine the origins of the dependence of the measured thermal resistance on these quantities. Studies of the use of d-c current gain as an indicator for the formation of hot-spots due to current constrictions were extended to higher current levels.

Microwave Device Measurements — Clamping of the waveguide system has been completed. Forces on the mixer (holder) far in excess of those required for diode ejection do not change the output voltage by more than 0.1 mV, as opposed to the several millivolt changes that were previously obtained with similar forces. The third micrometer-head stop was installed on the rotary-vane attenuator which had been modified to serve both as a modulator and modulation standard, and the attenuator was calibrated at the NBS Boulder Laboratories. An extensive and detailed review of a proposed IEC standard for mixer diode measurement methods was prepared and presented to the members of the microwave mixer and detector task group of the IEEE-GED Standards Committee for Electron Devices. The task group recommended that the U.S. National Committee oppose adoption of this standard. Comments to the appropriate military agencies were made on proposed changes of definitions and symbols for microwave diodes in MIL-S-19500, General Specification for Semiconductor Devices.

Carrier Transport in Junction Devices — A general explanation was developed to account for the previously reported significant differences in delay time as measured on different instruments or on the same instrument at different frequencies. Six R-C plug-in delay-time networks with time constants in the range 212 to 700 ps were fabricated for use in experiments to test this explanation and to characterize delay-time measuring instruments. Delay-time measurements were made with a Sandia bridge on several transistors and compared with measurements performed on the same transistors by another laboratory with a similar test system. S-parameter measurements were made on a type 2N2219 transistor; the base transit time obtained from an analysis of these measurements showed substantial agreement with the results of earlier measurements made with a vector-voltmeter test system. An analysis was completed to determine the delay-time error introduced into the vector-voltmeter test system by capacitive or inductive components in the test circuit collector-base impedance.

Standardization Activities — Many of the standardization activities undertaken by program staff are broader than the technical tasks described in the following sections. These activities involve general staff support in committees, coordination of

efforts which may encompass a variety of tasks, and participation in areas where no direct in-house technical effort is underway. Standardization activities directly related to particular task areas are reported with the appropriate tasks.

Although there was no meeting of ASTM Committee F-1 on Electronics during this quarter, program staff members reviewed editorially nine documents at the committee level and two documents at the subcommittee level. Three documents on leak detection were prepared. One, on leak detection by a helium mass spectrometer, was extensively revised. A first draft of a document on measurement of minority carrier diffusion length by the steady-state surface photovoltage technique was prepared. Revisions were made of the procedure for measuring carrier lifetime by photoconductive decay, and a round robin test was planned to test the effectiveness of the proposed changes. At the request of the Dielectrics Section of the committee, a procedure for measuring thickness of oxide and metal layers, prepared previously (NBS Tech. Note 475, p. 24), was circulated to section members for discussion at the January meeting.

A specification on glazed alumina substrate materials, prepared by SAE Committee H on Electronic Materials and Processes, was reviewed. Similarities and differences were identified between this specification and ASTM Specification D 2442 for Alumina Ceramics for Electrical and Electronic Applications at the fall meeting of the committee. Committee H is also concerned with plastic encapsulants, circuit boards, and other materials of particular interest to makers of hybrid microcircuits.

Tours of the Joint Program laboratory facilities were conducted in connection with the International Electron Devices Meeting in October and a meeting of the local section of the International Society for Hybrid Microelectronics in November. The program topic for the ISHM meeting was the NBS work on ultrasonic wire bond evaluation.

3. SIMICONDUCTOR MATERIALS

3.1. RESISTIVITY

Objective: To develop methods suitable for use throughout the electronics industry for measuring resistivity of bulk, epitaxial, and diffused silicon wafers.

Progress: Experimental study of the current and probe-force dependence of four-probe resistivity measurements was postponed in favor of work on statistical techniques to analyze the data acquired so far. The dependence of resistivity on measurement parameters has proven quite difficult to extract from measurement uncertainties. Work on the study by the surface photovoltage method of subsurface damage in silicon wafers due to processing was further deferred. A new interlaboratory test on epitaxial resistivity measured by the four-probe method was started following the termination of an earlier round robin when uncontrolled variations in an important test condition, probe force, were observed. Alternative polynomial representations for the temperature coefficient of resistivity of silicon near room temperature have been developed and prepared for review by ASTM Committee F-1 on Electronics. A modified collaborative reference program has been developed in response to the request by ASTM Committee F-1 that NBS supply silicon resistivity standards. The effort to disclose the source of visual linear defects in diffused silicon diodes which impaired the ability to make capacitance-voltage (C-V) measurements has been completed. The defects have not reappeared during any part of the investigation. Work to compare resistivity of silicon wafers as measured by the C-V and four-probe techniques shows that the doping density determined by the C-V method is 10 to 25 percent less than that derived from the four-probe measurement. The comparison is complicated by lack of a plateau value in most of the C-V based doping-density profiles. Comparison of C-V data on diffused wafers with measurements made by another laboratory indicates that difficulties in determining the capacitance of the diode in the presence of stray capacitances may be a major source of discrepancy.

Standardization Activities — Polynomial curve fit approximations to the temperature coefficient for silicon resistivity have been previously reported (NBS Tech. Note 560, pp. 6-7). The polynomials, thirteenth order for p-type and seventeenth order for n-type silicon, were judged by users to be too large to be handled conveniently, and considerable interest was expressed in alternative representations of the temperature coefficients. Study indicated that the only convenient alternative, comparable in accuracy of representation with the high order polynomials, required splitting of the resistivity range into two parts. In this manner, with an upper and a lower range for both p-type and n-type silicon overlapping slightly in the vicinity of 0.05 $\Omega \cdot$cm, it was possible to achieve adequate fits with fifth order

polynomials. It is expected that these partial fits would be most applicable to measurement situations in which a given test station is used for measurement of silicon in a limited resistivity range. The results have been summarized for discussion of their suitability at the January meeting of the section on resistivity of ASTM Committee F-1 on Electronics.

The round robin on four-probe measurements of the resistivity of silicon epitaxial layers deposited on opposite conductivity-type substrates that was being conducted in cooperation with ASTM Committee F-1 was terminated because uncontrolled variations in probe force, one of the test conditions, were observed. A second round robin has been started on this test method; an entire four-probe assembly with preset probe force is being circulated along with the test specimens. At the present time, two of the nine participants have completed measurements.

In response to a request for an NBS service to provide silicon resistivity standards for the electronics industry (NBS Tech. Note 560, pp. 10-11), detailed consideration has been given to a modified collaborative reference program format described previously (NBS Tech. Note 717, p. 7). Initial participation limited to about 12 laboratories is considered desirable both for manageability and for statistical sampling purposes. The resistivity values to be offered initially are 0.1 and 10 Ω·cm. Silicon with sufficient resistivity uniformity (radial variation 5 percent or less at half radius and 10 percent or less at 3.2 mm from the edge [1] and longitudinal variation 10 percent or less over a 150-mm crystal length) was found to be available in sufficient quantities to make replicate specimens available to all participants as resident standards. Pending favorable results, it is intended that the modified collaborative reference approach to resistivity standards would be replaced after about 18 months with a simplified procedure, direct sale of silicon wafer standards. A summary of the proposed approach has been prepared for presentation to ASTM Committee F-1 with a request for assistance from the committee in coordinating such a program.

(J. R. Ehrstein and F. H. Brewer)

Spreading Resistance Methods — Experimental difficulties were disclosed that limited use made of the scanning electron microscope (SEM) in the continuing investigation of probe damage on silicon wafers. High resolution pictures were obtained of deep damage pits at a magnification of 20,000 X using a beam accelarating potential of 20 kV. Later attempts to verify and expand these results were unsuccessful, 2000 X being the highest attainable magnification of the same specimen which retained reasonable clarity. The high resolution results were obtained immediately after a cleaning of the SEM. It appears from this and other considerations that the difficulty experienced in past SEM use on silicon specimens has been primarily due to

instrumental contamination and that the suitability of bulk silicon as a subject material no longer seems to be a point of question. (J. R. Ehrstein)

Capacitance-Voltage Methods — A final experiment was performed in the search to discover the origin of the linear defects observed on low quality diodes (NBS Tech. Notes 702, p. 8, and 717, pp. 8-10). Slices from 1.4- and 2.9-Ω·cm *n*-type silicon crystals and from the 12-Ω·cm *n*-type silicon crystal on which the defects were originally noticed were processed from sawing through planar diffusion. The linear defects previously observed were absent; the diode breakdown voltages were sufficiently near to the theoretical bulk breakdown value and the leakage currents were low enough to be quite suitable for making capacitance-voltage (C-V) measurements. Similar results were observed when four-probe resistivity profiles were made on the back of the 12-Ω·cm wafer; it had been thought that the damage from the probe points might be causing the defects, but this now appears unlikely. Since it has not been possible to induce similar defects in slices of the crystal on which they were originally noticed nor on slices of other silicon crystals processed through the same steps, it was concluded that neither the crystal nor the processing was responsible. The only change known to have been made since the initial observation of the defects was repair to the diamond wheel saw used to slice silicon crystals. While it is conceivable that damage caused by excessive vibration of the saw may have been the source of the defects, this hypothesis is not open to test and the search has been concluded.

(R. L. Mattis, T. F. Leedy, and M. Cosman)

Work continued on the experiment to compare resistivity values measured by the four-probe and junction C-V methods for a group of carefully selected specimens. Sets of *n*-type silicon slices with nominal resistivity of 0.1 and 30 Ω·cm have been added to the study. In the study C-V measurements are made on four or five diodes near the center of the slice. The first capacitance measurement on each diode is usually made at a forward bias of a few hundred millivolts. Successive readings are made at increasing reverse bias voltages chosen so that the capacitance is 90 to 95 percent of its previous value. The reverse bias voltage is increased until a value slightly less than the breakdown voltage is reached. The raw capacitance values are corrected for the small errors inherent in the meter.* The corrected capacitance values are smoothed by successive five point fits: that is, a linear fit is made of ln C *vs.* ln V for calibration-corrected data points 1 through 5, then for data points 2 through 6, etc.

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* The meter is calibrated periodically by making capacitance measurements on reference capacitors which have been calibrated by R. N. Jones of the NBS Electromagnetics Division.

A smoothed capacitance value and a slope, calculated from each five-point set, are used to compute the doping density profile.

At present, four-probe and C-V measurements have been completed on six bulk diffused slices. In general the doping profiles obtained from the C-V data are characterized by (1) a continuing increase in doping density with increasing depth and (2) a doping density which is usually less than that determined by the four-probe method before diffusion. The slope of the doping profile is reduced if an edge correction for diffused diodes reported by Wilson [1] is applied. The effect of this correction is generally to increase the difference between each C-V value and the four-probe value; it is most significant at large depletion depths. For 29 diodes profiled, and for depletion depths (corrected for edge effects) corresponding to reverse biases between about 2 V and breakdown (lower biases were omitted to reduce interference from the diffusion tail), the spread of doping densities in each of the various profiles was between 2.2 and 12.5 percent of the maximum doping density of that profile. The doping density determined by the C-V method ranged from 10 to 25 percent less than the four-probe value for these six slices. (R. L. Mattis and D. R. Ricks)

A comparison was made between C-V measurements made by NBS and by another laboratory. Two wafers, each with an array of planar diffused 20-mil (0.5-mm) diameter diodes, were fabricated by NBS, and three wafers, each with nine mesa diffused diodes approximately 12 mils (0.3 mm) in diameter, were fabricated by the other laboratory on wafers that had been polished and evaluated for radial resistivity variation by NBS. A common area was assumed for each diode, and all calculations were done at NBS. A doping density profile was made of a common diode from each wafer by both laboratories. In general, comparison of the doping density profiles generated by the two laboratories showed a different form of small scale disagreement for each wafer considered. However, if the data taken between 2 V reverse bias and breakdown voltage by the two laboratories are combined wafer by wafer, the spread of doping densities obtained for each wafer was between 5 and 35 percent of the maximum value for that wafer.

In a separate part of the comparison, five to nine mesa diodes on each of the three wafers were measured by both laboratories. A reverse bias voltage of 5 V was used throughout, and only corresponding capacitance values were compared. The nominal capacitance ranged from 3.9 to 17 pF. It was observed that (1) the capacitance measured by NBS was consistently larger than the capacitance measured by the other laboratory, (2) both the absolute and the relative differences were larger at lower values of capacitance, (3) the short term sample standard deviation of the NBS capacitance measurement, based on three successive measurements at the same bias voltage, was much less than the difference between laboratories, and (4) the short term

sample standard deviation of the capacitance measured by NBS was essentially the same for all three specimens.

This comparison between C-V measurements made by the two laboratories suggests that inter-laboratory capacitance measurements on diffused diodes are not likely to be reproducible to a desirable precison. This was made especially clear in the second phase of the comparison where the same bias voltage was used throughout. The problem could lie in differences in instrumentation, in stray impedances in series or parallel with the capacitance being measured, or in effects caused by trapping or interface states in the material. (R. L. Mattis)

Plans: Four-probe current and probe force studies are expected to resume with measurements on vapor-etched bulk slices of silicon. Further work will be done on statistical analysis of the data already acquired. Data will be reduced and tabulated as received from the four-probe epitaxial resistivity round robin. Scanning electron microscope studies of probe impact damage will continue when the microscope has been cleaned. The proposed silicon resistivity standards program will be presented to ASTM Committee F-1; subsequent developments will be determined by the committee response. The effect on capacitance-voltage measurements of series capacitance, possibly originating in the specimen back contact, will be considered. Comparisons between the four-probe and C-V methods will continue. Consideration will be given to using packaged commercial diodes for purposes of checking the equipment.

3.2. GOLD-DOPED SILICON

Objective: To characterize *n*- and *p*-type silicon doped with gold and to develop a model for the energy-level structure of gold-doped silicon which is suitable for use in predicting its characteristics.

Progress: Additional possible causes of the decrease of resistivity with increasing gold concentration in heavily gold-doped, *p*-type silicon were investigated. It was found that additional shallow acceptors were not being introduced unintentionally into wafers during gold diffusion so that this cause was eliminated from further consideration. Calculations based on a model that includes a shallow acceptor center coupled with the gold centers yield a resistivity dependence on gold concentration that agrees very well with experimental measurements on *p*-type, gold-doped silicon. Additional preliminary measurements of carrier lifetime were made by the surface photovoltage method in several *p*-type silicon wafers lightly doped with gold. Although the values obtained were generally in the same range as lifetime values calculated from capture cross section data in the literature, differences between the

measured and calculated values were observed. Possible causes of these differences are being investigated.

Resistivity Measurements — The experiment to determine whether shallow acceptor impurities, such as boron, are being unintentionally introduced during high temperature gold diffusions was completed. Four 10-Ω·cm *p*-type wafers were diffused at 1250°C for times of 8, 16, 32, and 64 h. Since the gold reaches its solid solubility concentration in 8 h, no further changes in gold concentration or in resistivity should occur with increasing diffusion times if gold is the only impurity affecting the electrical properties. Activation analysis results and electrical measurements on the set of four wafers showed that both the gold concentration and the resistivity were essentially the same for all wafers. The result of this experiment therefore indicates that observable amounts of additional shallow acceptor impurities are not being introduced during the high temperature gold diffusions, and suggests that this is not the cause of the decrease in resistivity of *p*-type wafers doped with large amounts of gold (NBS Tech. Note 702, pp. 9-11).

An analysis indicated that the introduction of an acceptor state between the valence band edge and the gold donor state with a concentration that depends on gold concentration can cause the observed decrease of resistivity as gold concentration increases. Such an acceptor state has recently been reported by Brückner [1] who observed an impurity state that is located 0.033 eV above the valence band and has suggested that it is an electrically active complex of gold with other defects. The concentration of these acceptors increases rapidly as the gold concentration increases. The results of calculations based on a solution to the charge balance equation to find the Fermi level and, hence, the hole concentration made with this impurity state added to the energy-level model for gold-doped silicon described previously (NBS Tech. Note 702, p. 9) are shown in figure 1. It was assumed that the acceptor concentration varies as the third power of the gold concentration and that the acceptor concentration is 4.5×10^{15} cm^{-3} at a gold concentration of 1×10^{17} cm^{-3}. Lattice mobility [2] and impurity mobility [3] were combined reciprocally to obtain the hole mobility used in the calculation of the resistivity. In these calculations the energy of the gold donor and acceptor state were taken as 0.35 eV above the valence band and 0.54 eV below the conduction band, respectively [4], the degeneracy factors were taken as 0.125 for the donor and 1.5 for the acceptor, and the energy gap and effective masses were taken from the work of Barber [5]. The agreement of the calculated curves to the data at low gold concentrations is sensitive to the degeneracy factor for the gold donor level. The value of 0.125 for the degeneracy factor gives a better fit to all three resistivity groups than either 0.25 or 0.0625. These values give significant shifts of the computed curves to the left and right, respectively,

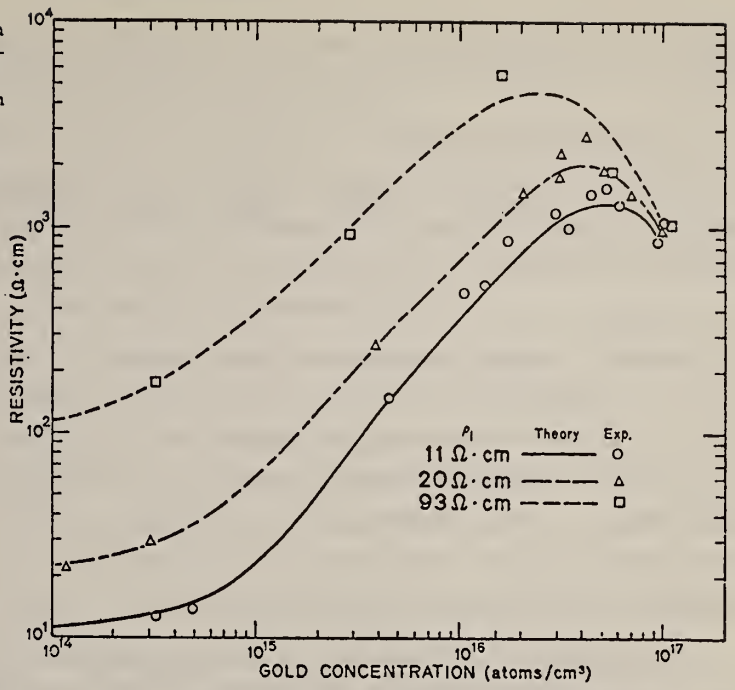

Figure 1. Resistivity as a function of gold concentration in p-type silicon with initial resistivity ρ_i of 11, 20, and 93 Ω·cm. (Error bars on the experimental points are not indicated. The standard deviation of the gold determination is estimated to be about 10 percent. Resistivity values are reproducible within about 5 percent. The parameters used to generate the theoretical curves are given in the text.)

of the experimental data. Exponential functions for the acceptor concentration can also be used to fit the experimental data. More knowledge about the origin of the acceptor center must be developed to aid in determining its true dependence on gold concentration.

A complicating factor in the analysis of the electrical data is the separation of the influence of the high temperature heat treatment from the effects of gold-doping. It is known that heat treatments can change the resistivity of silicon and that the presence of oxygen in a crystal produces donor levels when the material is heated to an appropriate temperature. Even though the diffusions are done at temperatures that are considered too high for donor formation, some changes may still occur. Diffusions have been made on oxygen-free silicon, but the oxygen present in the oxide surface layer may be driven in at high temperatures. Also most of the diffusions are made in an oxygen atmosphere. Control specimens without gold were included in many of the diffusions along with the specimens on which gold was evaporated. However, the control specimens did not remain free of gold, as confirmed by activation analysis data. A few control wafers were heated in the absence of any gold-containing specimens. Resistivity changes occurred, but contamination by gold on the walls of the diffusion tube can not be ruled out until activation analysis results are obtained on these specimens.

Resistivity measurements and neutron activation analyses were completed on the 2000 Ω·cm n- and p-type specimens diffused for very short times at 950 and 1150°C to study the effect of interstitial gold. Interpretation of these results awaits

completion of measurements on the sets of similar specimens diffused for longer times.

Resistivity measurements were completed on the specimens annealed at temperatures other than the diffusion temperature to study gold precipitation effects and on specimens heat treated without gold evaporations, but determinations of the gold concentrations by neutron activation analysis are still being made.

(W. R. Thurber, A. W. Stallings, J. Krawczyk, and W. M. Bullis)

Carrier Lifetime Measurements — Past studies of carrier lifetime in gold-doped silicon have generally been made by means of the reverse recovery technique in diodes [6, 7]. Because of uncertainties encountered in relating carrier lifetime in silicon diodes as measured by reverse recovery and open-circuit voltage decay and because of the desire to make measurements on gold-doped wafers without the necessity of forming *p-n* junctions, the steady-state surface photovoltage (SPV) method [8] was selected for use in the present work.

With the SPV method, either accurate or reproducible measurements of short diffusion lengths are much more difficult than measurements of long diffusion lengths. The standard deviation due to scatter in the data of an SPV plot is typically 0.5 μm, independent of diffusion length; the corresponding uncertainty in the value of the diffusion length is 1 to 2 μm. Thus the percentage error can be very significant for a diffusion length of 5 μm, while it is negligibly small for a diffusion length of 100 μm. The most obvious sources of error include noise and calibration uncertainty of the thermocouple detector and lock-in amplifiers, drift of the SPV signal with time, and incorrect values of the absorption coefficient and reflectivity.

Most of the measurements to date have been made on *p*-type specimens in the form of Hall bars. Specimen preparation consists of masking the side of the Hall bar containing the contacts and then removing about 25 μm from the other surface by a polishing chemical etch that consists of a mixture of nitric, hydrofluoric, and acetic acids. This treatment usually results in an SPV signal of a few millivolts which is adequate for the measurement.

In *p*-type silicon which the shallow acceptor concentration is much greater than the gold concentration the lifetime, τ, in seconds, is approximately

$$\tau = \frac{1}{\sigma_{e02} \, v_e \, N_{Au}}$$

where σ_{e02} is the capture cross section for electrons at the positively charged gold donor in square meters, v_e is the thermal velocity for electrons in meters per second, and N_{Au} is the gold concentration in atoms per cubic meter. The values for capture

Table 1 — Capture Cross Sections for Electrons and Holes in n-Type and p-Type Gold-Doped Silicon

	Capture Site	300 K (a)	(b)	(c)	(d)	162 K (e)	77 K (f)	(g)	
n-type									
σ_{e01}	Au^0	5	0.8	20	25	10	∿ 30	5	$\times 10^{-16}$ cm^2
σ_{h01}	Au^-	10	60		13	200	∿1000	2300	$\times 10^{-16}$ cm^2
p-type									
σ_{e02}	Au^+	35	31				∿ 600	1000	$\times 10^{-16}$ cm^2
σ_{h02}	Au^0	≥ 1	12				∿ 30		$\times 10^{-16}$ cm^2

a Bemski [9], from lifetime data. Calculated by the author assuming thermal velocities of about 1×10^7 cm/s.

b Fairfield and Gokhale [10], from capture probabilities obtained from photoconductivity decay measurements. Computed assuming a thermal velocity of 2×10^7 cm/s for both electrons and holes.

c Senechal and Basinski [11], from emission rate data. Calculated by the authors assuming $E_c - E_{Au} = 0.545$ eV, $v_e \simeq 2\times10^7$ cm/s, and a degeneracy factor for the gold level of unity. The value at 300 K is based on the authors' extrapolation of data obtained at 250 K to room temperature.

d Tasch and Sah [12], from emission rate data. Calculated by the authors assuming $E_c - E_{Au} = 0.545$ eV, $E_{Au} - E_v = 0.588$ eV, and thermal velocities of about 2×10^7 cm/s. The degeneracy factors were arbitrarily assigned a value of unity.

e Colligan and van Vliet [13], from measurements of generation-recombination noise. Calculated by the authors but the values used for the thermal velocities could not be extracted.

f Davis [14], from lifetime measurements using alpha particle irradiation. Calculated by the author assuming thermal velocities of 1.3×10^7 cm/s for electrons and 1.0×10^7 cm/s for holes.

g Bemski [9]. Computed from 300 K values using temperature dependence given. No temperature dependence was quoted for σ_{h02}.

Table 2 — Measured and Calculated Minority Carrier Lifetimes in p-Type Gold-Doped Silicon

Specimen Number	ρ_i ($\Omega\cdot$cm)	ρ_f ($\Omega\cdot$cm)	Gold Conc. (atoms/cm^3)	L (μm)	D (cm^2/s)	τ(ns) Measured	τ(ns) Calculated
10P850-288	11	13.5	4.9×10^{14}	9	35	23	33
10P950-144	11	147	4.5×10^{15}	2.3	35	1.5	*
20P850-32	20	21.5	1.2×10^{14}	28.5	35	232	134
20P850-288	20	29.5	3.1×10^{14}	14.8	35	63	52

* Not calculated because the gold concentration exceeds the shallow acceptor concentration.

cross sections in gold-doped silicon reported in the literature are compiled in table 1. For the positive gold donor, the cross sections found by Bemski [9] and by Fairfield and Gokhale [10] are in better agreement then for the other centers. Lifetimes calculated using a cross section of 3.1×10^{-19} m^2 and a thermal velocity of 2×10^5 m/s are compared in table 2 with the lifetime values computed from the measured diffusion lengths of the gold-doped specimens. Measurements on more specimens are needed before definite conclusions can be reached regarding the dependence of lifetime on gold concentration or the appropriateness of the available cross section data.

(W. R. Thurber, W. E. Phillips, and W. M. Bullis)

Plans: Gold diffusions, which have been started on sets of *p*-type wafers with initial resistivity of 0.08, 1, 300, and 2400 Ω·cm, will be completed. Resistivity and Hall effect measurements at room temperature are in progress on 0.5-, 1000-, and 2000-Ω·cm gold-diffused *p*-type material and will be finished. Measurements will be completed on the specimens in the studies of high-temperature heat treatment, interstitial gold, and precipitated gold. Following analysis of the data, additional experiments may be planned. Hall effect and resistivity will be measured as a function of temperature on selected gold-doped silicon specimens to gain information on the nature of the shallow acceptor states which appear to be influencing the resistivity at high gold concentrations.

Some additional improvements to the surface photovoltage system are scheduled; these are expected to increase the ease and speed with which measurements can be made. Once these are complete, measurement activity will be increased in order to collect the information necessary to resolve the conflicts in published capture cross section data.

Investigation of the relationship between the reverse recovery and voltage decay methods for measuring carrier lifetime in silicon diodes will be resumed in order to develop the capabilities necessary to extend the study of gold-doped silicon to junction structures.

3.3. INFRARED METHODS

Objective: To study infrared methods for detecting and counting impurity and defect centers in semiconductors and, in particular, to evaluate the suitability of the infrared response technique for this purpose.

Progress: Some insight has been gained as to the mechanism of the infrared response (IRR) of germanium and silicon *p-i-n* diodes with wide *i*-regions. The effect appears to be that of the impurity photo-EMF observed in *p-n* diodes. The IRR of a

neutron-irradiated lithium-drifted germanium diode showed enhancement of certain features in the spectrum. The IRR of four commercial lithium-drifted silicon detectors has been measured. A variety of features was observed in the spectra on unirradiated specimens and on neutron-, proton-, and electron-irradiated specimens; the observed features are being interpreted in terms of defect states.

Infrared Response Mechanism — A review of the literature on measurements of energy states arising from the presence of defects and impurities in semiconductors by photoconductivity and related techniques has suggested that the steady-state photo-EMF, or photovoltage, established when minority carriers are generated by illumination is probably the basic mechanism for the IRR in p-i-n diodes with wide i-regions. Two phenomena associated with this photovoltage effect are in agreement with the IRR results.

Firstly, light in the impurity wavelength region (energy less than the bandgap energy) transfers electrons from filled energy states to the conduction band so that the equilibrium between the states and the valence band is upset. Equilibrium is reestablished by further optically-induced electron transitions from the valence band to these states. These double-optical transitions are possible only if the energy of the light is greater than one-half the bandgap energy of the semiconductor [1]. In the IRR measurement, no spectral features that can be linked to impurity or defect states have been seen at energies less than one-half the bandgap energy.

Secondly, preliminary excitation of the specimen with radiation in the intrinsic absorption region (energy equal to or greater than the bandgap energy) can produce over-population of impurity states leading to the observation of an impurity photovoltage [1]. In the IRR measurement on germanium diodes, the use of a 1-mm thick germanium filter results in an enhancement of the details observed in the spectrum as compared with those observed with the use of a thicker filter. This effect is related to the observed increase in radiation of energy near the bandgap energy transmitted by the thinner filter (NBS Tech. Note 592, pp. 23-25) [2].

Even though the impurity photovoltage spectrum is only observed at energies greater than one-half the bandgap energy, it is possible to observe energy states which lie in both halves of the forbidden gap. The photovoltage is observed if the photon energy exceeds the energy difference between the state through which excitation is occurring and the edge of the conduction or valence band, whichever is greater [3]. (A. H. Sher)

Infrared Response Measurements on Germanium — The IRR of five lithium-drifted germanium diodes was measured during this quarter. Of particular interest was NBS-83-8, fabricated from a portion of the same crystal as NBS-83-3 (NBS Tech. Notes 598, pp. 14-15, and 717, pp. 13-14). The portion of the crystal from which NBS-83-8 was fabricated

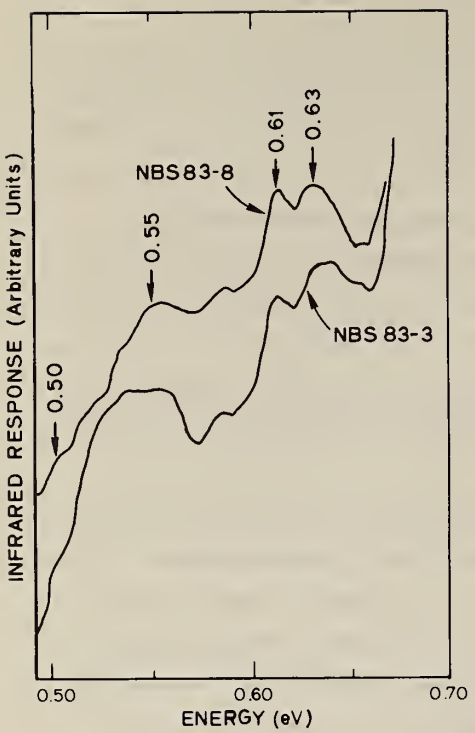

Figure 2. Infrared response spectra of two germanium gamma-ray detectors.

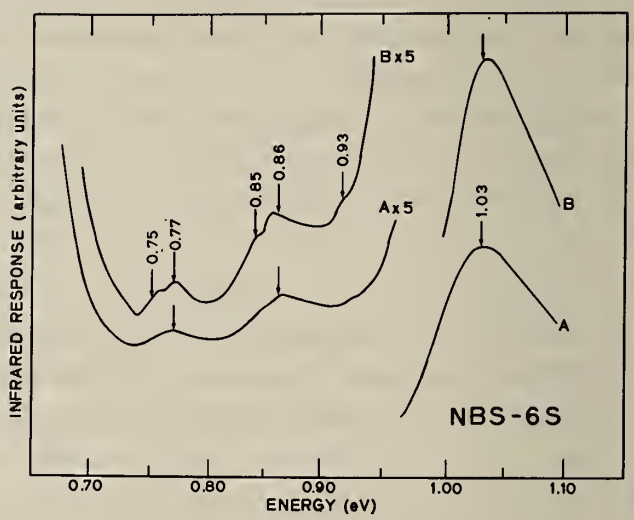

Figure 3. Infrared response spectra of a commercial lithium-drifted silicon detector obtained before (A) and after (B) irradiation with fast neutrons.

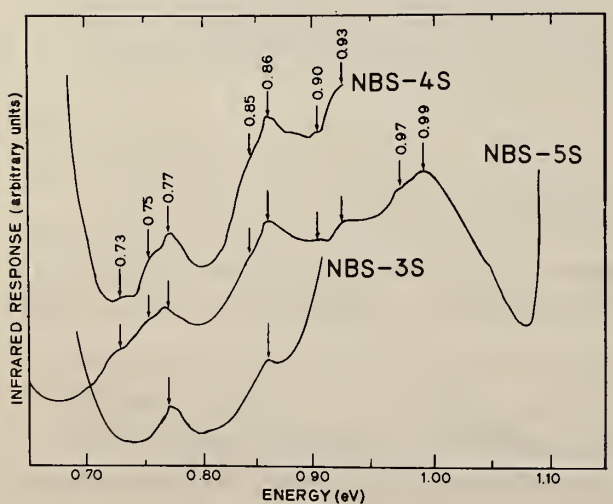

Figure 4. Infrared response spectra of three commercial lithium-drifted silicon detectors. (Large peaks, similar to that in the spectrum of NBS-6S shown in figure 3, occur at 1.03 eV in the spectra of NBS-3S and NBS-4S. These are not shown because they exceed the scale of the figure.)

had been irradiated with neutrons at a fluence of approximately 1.3×10^{10} cm^{-2}. The IRR spectra of NBS-83-3 and NBS-83-8 are shown in figure 2. It is evident that features in the spectrum of NBS-83-8 at energies of 0.55, 0.61, and 0.63 eV are enhanced over those in the spectrum of NBS-83-3. The other features of the spectrum of NBS-83-3 appear to be preserved in the spectrum of NBS-83-8.

In studying radiation-damaged material, possible annealing effects must be considered. A published study of high-temperature annealing of defects produced by neutron irradiation of germanium [4] at fluences in the range 10^{15} to 10^{16} cm^{-2} is particularly appropriate to the present case as the temperature range studied includes the temperatures employed in the lithium-drifted diode fabrication process. After irradiation four energy states were reported to be located at 0.01, 0.07, and 0.17 eV above the valence band and 0.20 eV below the conduction band. After annealing, a new level 0.10 eV below the conduction band was observed. With the exception of the state located 0.01 eV above the valence band which is not within the energy range shown in figure 2, these states correspond to the features labeled in the figure.

Infrared Response Measurements on Silicon — Measurements of IRR on lithium-drifted silicon detectors continued. Efforts to correlate features observed in the IRR spectra with known defects in silicon have been hampered somewhat by the lack of agreement on the value of the energy states of such defects in the literature. For example, energy states given for the divacancy in two recent studies appear to differ by as much as 25 percent [5, 6]. For identification purposes, features which are observed in the IRR measurements are associated with energy states that have been reported in the literature; the IRR method has not been used as yet in order to determine the defect from which the observed state arises.

Figure 3 shows IRR spectra, obtained using a 0.14-mm thick silicon filter, of a lithium-drifted silicon detector before and after irradiation with fast neutrons through the *p*-contact at a fluence of 5×10^{9} cm^{-2}. As might be expected for such a fluence the two spectra are virtually identical. However, the peaks at 0.86 and 0.77 eV are somewhat enhanced, and the feature at 0.93 eV is much enhanced after irradiation. The two lower energy peaks are associated with states located 0.40 eV below the conduction band (0.77 eV) and 0.31 eV above the valence band (0.86 eV) previously reported from observations of photoconductivity on silicon specimens irradiated with neutrons at fluences from 1×10^{16} to 5×10^{19} cm^{-2} and attributed to divacancies [5].

Figure 4 shows IRR spectra obtained from three commercial lithium-drifted silicon detectors presumed to be fabricated from specimens of the same silicon crystal. NBS-3S was not irradiated, NBS-4S was irradiated with 1.9 MeV protons at a fluence of 1×10^{14} cm^{-2} incident on the *p*-contact, and NBS-5S was irradiated with 1.5-MeV

electrons at a fluence of approximately 3×10^{13} cm^{-2} incident on the p-contact. The spectra of NBS-3S and NBS-4S are similar as might be expected since damage caused by 1.9-MeV protons should be localized outside the sensitive region of the device. As in the case of NBS-6S (figure 3), the main features are observed at 0.77 and 0.86 eV, and 1.03 eV. The IRR spectrum of the electron-irradiated specimen, NBS-5S, shows features at 0.99, and 0.90 eV as well as those at 0.93, 0.86, and 0.77 eV observed in the other silicon diodes. In the literature, a state located 0.18 eV below the conduction band (0.99 eV) arising from the vacancy-oxygen complex has been reported [7], while a state 0.27 eV above the valence (0.90 eV) may be associated with lithium precipitates [8]. (A. H. Sher, Y. M. Liu, and W. J. Keery)

Plans: The intensive review of photoconductivity literature as well as of related effects such as impurity photovoltage in germanium and silicon will continue. The studies of IRR on germanium and silicon diodes will continue. Efforts to extend the IRR technique to transistors and diodes will continue. Results of the IRR measurements on radiation-damaged silicon detectors will be prepared for publication.

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4. SEMICONDUCTOR PROCESS CONTROL

4.1. DIE ATTACHMENT EVALUATION

Objective: To evaluate methods for detecting poor die attachment in semiconductor devices with initial emphasis on the determination of the applicability of thermal measurements to this problem.

Progress: Experimental investigations were completed in the evaluation of the applicability of thermal response measurements to the detection of voids in diode die attachment. Previous measurements (NBS Tech. Note 717, pp. 19-22) indicated that, for the diode structure being studied, the transient thermal response was approximately three times as sensitive to the presence of voids in the die attachment as the steady-state thermal response or thermal resistance. It was concluded that the transient thermal response technique demonstrated sufficient sensitivity in diode structures that investigation of its applicability to the detection of voids in die attachment of transistor structures should be initiated. The earlier work on diodes also has shown that sensitivity to void sizes of both 20 and 40 percent of the chip bonding area was nearly the same. A theoretical study of the heat flow pattern in diodes with voids was begun in an attempt to understand the similarity of response in diodes with void areas of these sizes. In a search for means for simplifying the measurement it was found that the temperature coefficient of the forward voltage drop was essentially constant for a given lot of devices so that it is not necessary to measure this quantity for each device in a lot.

Diodes — Two new lots of diodes were fabricated to study the effects of (1) case thermal conductance and (2) void location on the transient thermal response measurement. Eleven diodes (Lot N) were bonded to special, solid-steel TO-5 headers each with a 20-mil (0.51-mm) diameter dimple to produce a 20-percent centrally located void area. Nine diodes (Lot P) were bonded to standard iron-nickel-cobalt alloy, glass-backed TO-5 headers each with two 14-mil (0.35-mm) diameter dimples to produce a 20-percent off-center void area. Nine control diodes were bonded to headers of each type without dimples.

For the transient thermal response measurements the heating power pulse width was 10 ms. The diode heating current was 800 mA for the transient measurements and 300 mA for the steady-state measurements except in the case of the group N devices where it was necessary to increase the steady-state heating current to 500 mA in order to maintain the 15°C increase in junction temperature in the control group. The temperature sensitive parameter was measured 50 μs after the termination of the heating power pulse with a measuring current of 5 mA.

The results obtained on these groups are summarized in table 3 together with results previously obtained on a group of nine diodes (Lot L) bonded to standard iron-nickel-cobalt alloy, glass-backed TO-5 headers each with a single 20-mil (0.51-mm) diameter dimple to produce a centrally located 20-percent void area and their control group of ten diodes. The first group of entries gives the junction-to-case temperature difference measured under steady-state conditions for the control-diodes [ΔT_{ss} (controls)] and the diodes with voids [ΔT_{ss} (voids)]. The third line is the increase in the average junction-to-case temperature difference of the voided devices over that of their controls expressed as a percentage of the latter. The range given is one sample standard deviation. The second group of entries gives the junction-to-case temperature difference measured under transient conditions for the control-diodes [ΔT_t (controls)] and the diodes with voids [ΔT_t (voids)]. The third line of this group is the increase in the average junction-to-case temperature difference of the voided devices over that of their controls expressed as a percentage of the latter. Again, the range given is one sample standard deviation. The last line of the table gives the difference between the percent increase obtained for transient response measurement and that obtained for steady-state response measurements expressed as a percentage of the latter. This quantity represents the percent increase in sensitivity to voids of transient response over that of steady-state response. Except where otherwise noted each sample group consisted of nine diodes.

Comparison of the data for the diodes in Lot N with that for diodes in Lot L leads to the following observations. As noted above, the heating current to produce a given increase in steady-state junction temperature is larger for the Lot N diodes; this occurs because of the larger thermal conductivity of the steel (approximately 2.5 times that of the iron-nickel-cobalt alloy) and the correspondingly lower thermal resistance of the Lot N diodes (32°C/W) as compared with the Lot L diodes (56°C/W). The difference in increase in junction temperature for a constant heating current level in the transient response case was significantly less for the control diodes of the two lots than for the diodes with voids; this indicates that the case characteristics are reasonably well decoupled from the transient thermal response as measured after a 10-ms wide power pulse. Nevertheless the sensitivity of the thermal response to voids in the Lot N diodes is considerably below that of the Lot L diodes. This probably results from the much greater thermal diffusivity (ratio of the thermal conductivity to the product of the mass density and heat capacity) of steel as compared with the iron-nickel-cobalt alloy. It has been reported that the peak junction temperature for devices operating with hot spots under pulsed operation is strongly dependent on the thermal diffusivity of the header material below the silicon chip [1] because a material with higher thermal conductivity and lower heat capacity is better able to transfer the heat away from areas adjacent to the silicon chip, thus decreasing the temperature of the hot spots.

Table 3 — Comparison of Results of Junction-To-Case Temperature Difference Measurements for Devices with 20 Percent Chip-Void Area

Lot No.	L	N	P
ΔT_{ss} (controls) (°C)	15.58±0.48[a]	14.89±0.57	14.91±0.27
ΔT_{ss} (voids) (°C)	16.93±0.35	16.21±0.89[b]	16.35±0.86
% increase	8.7±3.8	8.9±7.1	9.7±6.1
ΔT_t (controls) (°C)	11.74±0.49[a]	11.19±0.42	11.80±0.48
ΔT_t (voids) (°C)	15.66±0.63	13.75±0.85[b]	14.95±1.49
% increase	33.4±7.0	22.9±8.5	26.7±13.3
% difference (t-ss)	284	157	175

Lot L iron-nickel-cobalt case, centered void
Lot N steel case, centered void
Lot P iron-nickel-cobalt case, two off-center voids

[a] 10 diodes
[b] 11 diodes

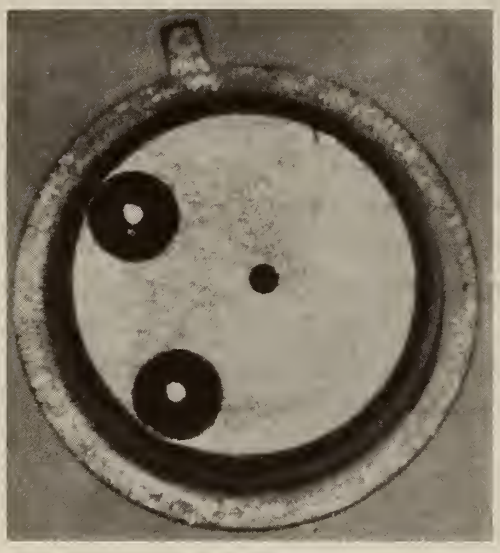
Table 4 — Measurements to Determine Reproducibility of the Die Attachment Evaluation Equipment

Device No.	TRANSIENT RESPONSE ΔT_{JC} (°C)	TRANSIENT RESPONSE $\Delta T_{JC}/P$ (°C/W)	STEADY-STATE RESPONSE ΔT_{JC} (°C)	STEADY-STATE RESPONSE $R_{\theta JC}$ (°C/W)
	(Average value and sample standard deviation)			
P1	14.85±0.17	12.90±0.11	15.04±0.31	54.08±1.11
P4	14.25±0.24	12.72±0.20	15.32±0.38	55.81±1.31
P5	15.03±0.28	13.30±0.28	15.24±0.37	55.12±1.37
P6	15.45±0.22	13.59±0.23	15.14±0.38	54.59±1.40
	(Percent relative sample standard deviation)			
P1	1.14	0.85	2.06	2.05
P4	1.75	1.57	2.48	2.35
P5	1.86	2.11	2.43	2.49
P6	1.42	1.69	2.51	2.56

Comparison of the data for the diodes in Lot P with that for diodes in Lot L suggests that the sensitivity of the thermal response to voids depends on the details of void location and geometrical arrangement. The sensitivity of the steady-state thermal response to voids was substantially lower but essentially the same for both lots, and so apparently it is not sensitive to these details.

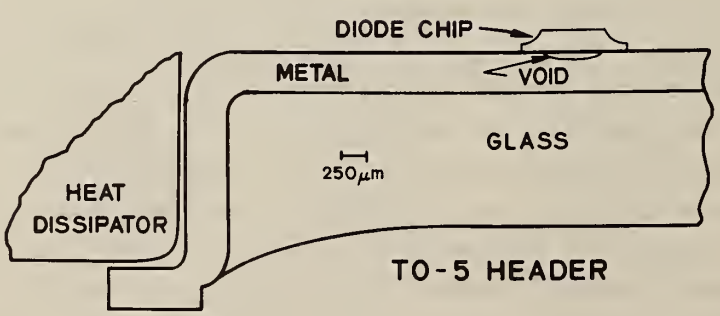
Additional long-term, single-operator thermal response measurements were made on four diode chips, of the same type as used in the above experiments, bonded to standard iron-nickel-cobalt alloy, glass-backed TO-5 headers without voids. Over a period of 10 days, steady-state and transient thermal response for a heating-power pulse width of 10 ms were measured 18 times on each diode. The diode forward voltage drop during heating was also measured to permit thermal resistance and transient thermal response normalized to heating power to be calculated. The average value, sample standard deviation, and relative sample standard deviation of the thermal response (junction-to-case temperature difference, ΔT_{JC}), the transient thermal response normalized to heating power, ($\Delta T_{JC}/P$), and the junction-to-case thermal resistance ($R_{\theta JC}$) obtained for each measurement condition are listed in table 4. The diode heating current was 1.0 A for the pulsed measurements and 300 mA for the steady-state measurements. In all cases the diode forward voltage drop, the temperature sensitive parameter, was measured 50 μs after the termination of the heating current. The maximum sample standard deviations for the steady-state and transient thermal response measurements of 0.38 and 0.28°C, respectively, while slightly larger than values reported previously (NBS Tech. Note 702, pp. 15-17), lie within an acceptable range for the instrument in the present application. The data also indicate that under conditions of equal ΔT_{JC}, the sample standard deviations of the pulsed measurements were less than those of the steady-state response measurements. Since the percent relative sample standard deviation was essentially the same for the thermal response and normalized thermal response (or thermal resistance) measurements it is concluded that for the device type under investigation either transient thermal response or transient thermal response normalized to heating power can be measured with no difference in reproducibility. This occurs because, for the conditions of measurement on this type of diodes, the heating power is maintained constant to within a percent or so by maintaining the heating current constant. For devices where this is not the case it is necessary to compare thermal response normalized to heating power rather than thermal response.

Analysis — A study was undertaken to determine why, for the diode chip-case system under investigation, the diode thermal response was essentially the same for void areas of both 20 and 40 percent (NBS Tech. Note 717, pp. 19-21). The diode chip-case system is shown in figure 5. A photomicrograph of the glass-backed iron-nickel-cobalt alloy TO-5 header with a 20-mil (0.51-mm) diameter dimple machined into it is shown in figure



a. Photomicrograph of TO-5 header with 20-mil (0.51-mm) diameter dimple. Magnification ∿6.4 X.

b. Photomicrograph of TO-5 header with 40-mil (1.02-mm) square diode chip bonded over dimple. Magnification ∿6.4 X.



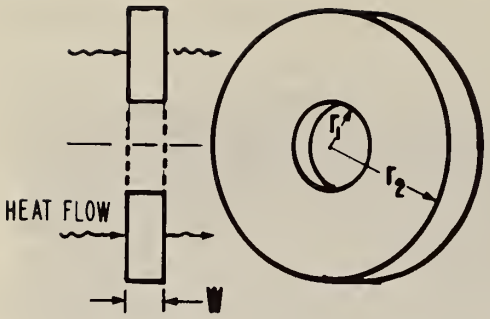
c. Cross-sectional view of diode chip bonded to header.

Figure 5. Diode with controlled void.

5a. A commercially available 40-mil (1.02-mm) square mesa diode is shown bonded to the header in figure 5b, and a scaled sectional view of the completed structure is presented in figure 5c. If it is assumed that all the heat is removed from the diode p-n junction by conduction through the case to the heat dissipator, then the effect of a void on the junction temperature is mainly dependent on what path the heat takes. Since the glass backing of the TO-5 header has a thermal conductivity, κ, much smaller than that of the alloy shell it can be assumed that the heat from the diode chip is confined mainly to the metal shell. A preliminary analysis of the heat flow was made by considering two extreme models for the chip-case interface region. For the one-dimensional model depicted in figure 6a, the thermal resistance increases with increasing washer hole or void size. For the case when the heat flow changes direction by 90 deg at the interface as depicted in figure 6b, the thermal resistance decreases with increasing washer hole or void size. The actual heat flow path is probably a combination of the two extremes depicted. It is therefore evident that the effect of a void of increasing size in the die attachment of a device bonded to a TO-5 header can cause the junction-to-case thermal resistance to increase, decrease, or remain unchanged depending on the relative weighting factors associated with the heat flow paths involved.

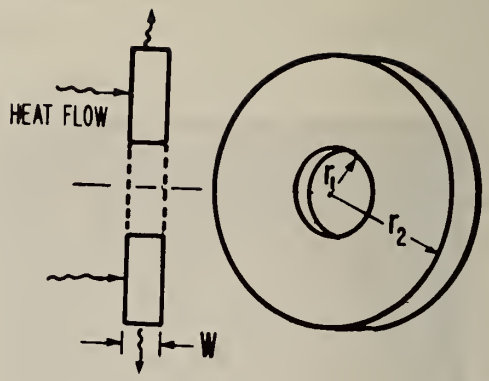
Industrial Screening Method — A study was undertaken to simplify the transient thermal response measurement procedure and make it less time consuming for use as a manufacturing screen or process control measurement. If it is assumed that the temperature coefficient of the temperature sensitive parameter is the same for all members of a given group of devices of the same type or lot, it is possible to eliminate conversion of the temperature sensitive parameter to temperature in the calculations. This assumption has been reported to be generally valid for semiconductor devices where the forward voltage of a p-n junction is used as the temperature sensitive parameter [2]. In a test of this assumption for the diodes under investigation it was found that the percent relative standard deviation of the temperature coefficient of the forward voltage for three lots of devices was less than 1.0 percent of the average value for the lot and so the assumption of constancy is in fact justified for this type of diode.

If it can be assumed that the power dissipation in the diodes is the same for a constant heating current, then it is necessary only to measure the diode forward voltage first under conditions of no internal power dissipation and then at some specified time after the termination of the constant-current heating power pulse. A quantity proportional to the junction-to-case temperature difference is obtained by subtracting the second voltage from the first. A typical circuit for measuring these forward voltages is shown in figure 7. The circuit is controlled by a clock pulse with adjustable



$$R_\theta = \frac{W}{4\pi\kappa}\left(\frac{4}{r_2^2 - r_1^2}\right)$$

a. One dimensional.



$$R_\theta = \frac{1}{4\pi\kappa W}\left[\frac{1}{2} - \left(\frac{r_1^2}{r_2^2 - r_1^2}\right)\ln\left(\frac{r_2}{r_1}\right)\right]$$

b. Two dimensional.

Figure 6. Models for heat flow patterns.

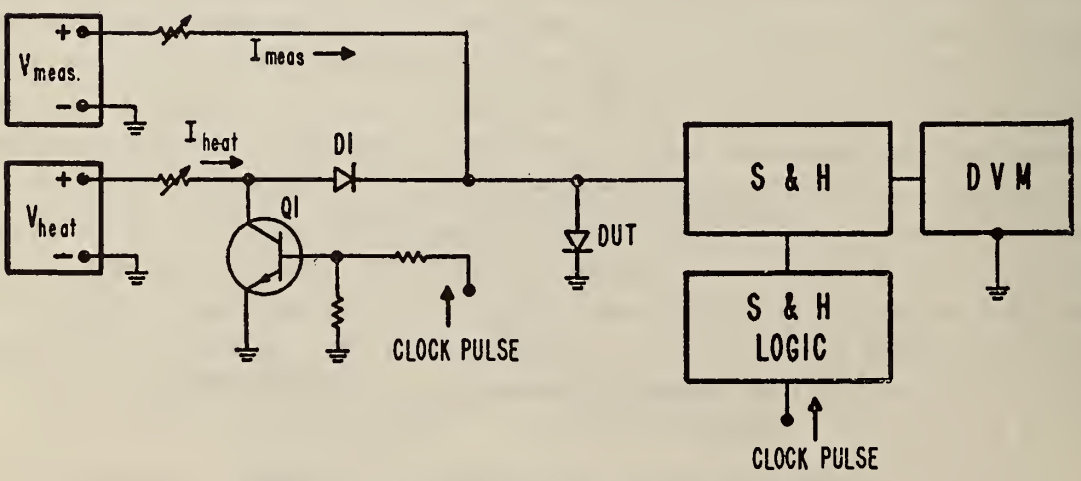


Figure 7. Thermal response measurement system.

width and repetition rate. When the voltage level of the clock pulse is zero, the transistor Q1 is off and the current through the diode under test is the sum of I_{heat} and I_{meas}. For the diodes under investigation, it has been found convenient to maintain I_{heat} at a constant level in the range 0.6 to 1.0 A for about 10 ms and to maintain I_{meas} at a constant level of 5 mA. At the end of the desired heating power pulse the clock pulse assumes a level of about +5 V for a period of time long compared with the heating interval. This is sufficient to bias the transistor Q1 on, which reverse biases the diode D1 so that I_{heat} no longer passes through the diode under test. After a delay, usually 50 μs, the sample-and-hold unit senses the diode forward voltage drop for a 1.5-μs period and displays it on the digital voltmeter. The two required voltages are obtained by first making a measurement with the heating current supply disconnected and then connecting the heating current supply and making the measurement in the manner described above.

By switching the sample-and-hold unit to sense on the negative slope of the clock pulse, it is also possible to measure the forward voltage drop during the heating period. This quantity can be combined with the heating current to obtain heating power which is needed if it is desired to normalize the thermal response to heating power.

Transistors — Study of the application of the transient thermal response technique to the identification of voids in transistor die attachment began with investigation of the various diode operating modes of a transistor to determine which, if any, are sufficiently sensitive to voids at attainable levels of heating current.

(F. F. Oettinger and R. L. Gladhill)

Plans: The analysis of heat flow to determine the limitations of thermal response techniques for detecting poor die adhesion in the diodes under investigation will continue. Experiments to apply the transient thermal response technique to transistors with poor die adhesion will be continued.

4.2. WIRE BOND EVALUATION

Objective: To survey and evaluate methods for characterizing wire bond systems in semiconductor devices and, where necessary, to improve existing methods or develop new methods in order to detect more reliably those bonds which will eventually fail.

Progesss: Several devices that had been power cycled 76,000 times at the Marshall Space Flight Center were examined with a scanning electron microscope; it was observed that, even though there were no failures, bond deterioration was pronounced in cases where the bond deformation was greater than two diameters. In continuing work on

Figure 8. SEM photomicrographs of ultrasonic aluminum wire bonds made with large loop heights showing variation in bond deformation. (At the time of the SEM observations the transistors had endured 76,000 power cycles. The hillock growth on the aluminum metallization is a result of the power cycling.)

a. Small bond deformation (∿1.2 times wire diameter). Magnification ∿585 X.

b. Average bond deformation (∿1.6 times wire diameter as determined from head-on SEM photomicrograph). Magnification ∿460 X.

c. Large bond deformation (∿2.2 times wire diameter as determined from head-on SEM photomicrograph). Magnification ∿230 X.

ultrasonic bonding of aluminum ribbon wire it has been found that alteration of the bonding schedule from the normal short-time, high-power conditions to longer time, lower power conditions improves the cosmetic appearance, increases the bond strength, and eliminates the heel crack. Measurement techniques were improved for the in-process study of ultrasonic wire bonding. In addition, a new modification of the bonding schedule, termed phased-burst bonding, has been introduced. Use of this schedule appears to result in increased bond adherence. Preliminary information has been developed that provides insight into the mechanisms of ultrasonic bonding. One significant finding is that it does not appear to be necessary for the tool to grip the wire and move it across the substrate metallization to make the bond. Experimental and statistical analysis of significant factors in the wire bond pull test continued with investigations of the effect of the angle between pull force and the bond wire on the measured pull strength.

Bond Failure from Slow Thermal Cycling — The results of calculations have shown that an increased loop height would be expected to minimize wire bond flexure during slow power cycling, and increase the life of the device (NBS Tech. Note 717, pp. 23-25). Observations were carried out with a scanning electron microscope (SEM) on a sampling of transistors that had been fabricated with loop heights in the range 300 to 375 μm (0.012 to 0.015 in.), significantly higher than normal, and then subjected to thermal cycling at the NASA Marshall Space Flight Center. Five devices, part of a lot of 100 transistors that had been cycled 76,000 times with no failures, were examined.

There was considerable variability in the deformation of the wire bonds to the semiconductor dice. Based on the observation of 10 such bonds, it appeared that bond deterioration such as heel cracking and loss of material in the center of the bond was pronounced where the bond deformation was greater than about two wire diameters. Typical examples are shown in the SEM photomicrographs in figure 8. Despite the severe bond deterioration observed in some cases, the remaining 95 devices of the original group have withstood 25,000 additional power cycles without failure. The long life of these devices confirms that high loop height reduced flexure fatigue; in earlier groups, failure began to occur from a few hundred to a few thousand cycles.

The metallization hillocks seen in the SEM photomicrographs are a normal result of such power cycling [1, 2]. The hillock growth apparently results from creep of the aluminum in the metallization and bears a strong visual resemblance to that resulting from electromigration [2, 3]. If the growth mechanism is the same, then hillock growth should be inhibited by the same methods that are reported to be successful in retarding electromigration, such as doping the metallization [4].

(W. E. Phillips, K. O. Leedy, and G. G. Harman)

A WIRE CLAMP
B TRACKS
C MOVABLE STAGE
D HORIZONTAL ADJUSTMENT
E ROTATING BASE
F BONDING ADJUSTMENT
G BONDING TOOL

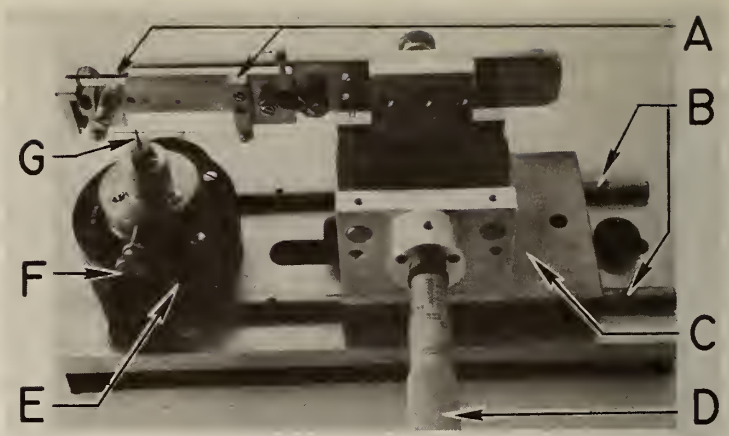


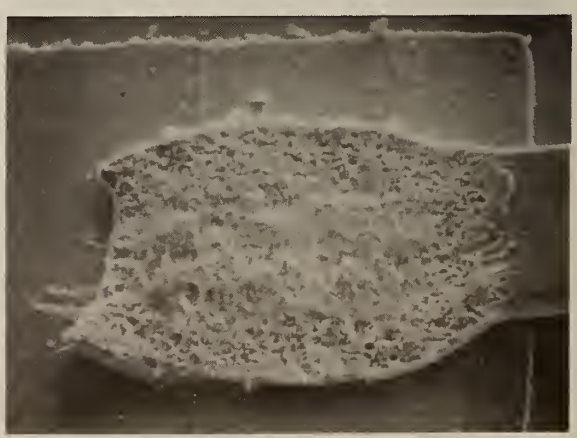
Figure 9. Device for polishing convex surfaces and grooves on bonding tools.

a. First bond. Magnification ∿460 x.

b. Second bond. Magnification ∿470 x.

Figure 10. SEM photomicrographs of ribbon wire bonds made with low power [20-μin. (0.5-μm) peak-to-peak tool tip amplitude] and long time [155 ms].

a. First bond. Magnification ∿430 x.



b. Second bond. Magnification ∿500 x.

Figure 11. SEM photomicrographs of ribbon wire bonds made with normal power [82-μin. (2.7-μm) peak-to-peak tool tip amplitude] and time [40 ms].

Ribbon-Wire Bonding — Work on ultrasonic bonding of aluminum ribbon wire equivalent in cross-sectional area to 0.001-in. (25-μm) diameter round wire has continued. The order for varying sizes and metallurgical composition of ribbon wire, placed last quarter, had to be cancelled because the manufacturer, who has supplied such wire in the past, encountered equipment and other problems with dimensional control. Fortunately, two other wire manufacturers have expressed interest in producing ribbon wire and one has supplied samples with excellent dimensional characteristics.

Construction has been completed on a device for producing convex surfaces and grooves on the bottom of bonding tools. Such variations in bonding tool shape are necessary to determine designs that produce the strongest ribbon-wire bonds. The device, pictured in figure 9, consists of a rotating base on which the bonding tool is clamped. Adjustment is provided in both the vertical and horizontal directions. A small wire of the desired shape mounted in the clamp is loaded with diamond-bort paste. The clamp is attached to a stage that can be moved on the tracks so that the wire is drawn back and forth across the tool face. (A. W. Stallings and H. K. Kessler)

About 2000 bonds were made on several single-level bonding substrates in order to investigate the pull strength and cosmetic appearance resulting from changing the bonding power and time. The bonding force was held constant at 25 gf (245 mN) throughout the investigation. The wire was aluminum (1% silicon) with a tensile strength of 12 to 14 gf (118 to 137 mN) and cross sectional dimensions of 0.0005 by 0.0015 in. (13 by 38 μm). The bond length was 0.040 in. (1 mm), similar to that used in typical devices. The same tool was used for all tests. SEM photomicrographs of typical bonds selected from this study are shown in figures 10 to 13.

A better cosmetic appearance was obtained with low ultrasonic power and relatively long bonding time (figure 10) than with the more conventional higher ultrasonic power and shorter bonding time. In the latter case, the bond surface appearance is rough and irregular, and a significant heel crack appears in the first bond (figure 11). In addition, it had been observed previously (NBS Tech. Note 702, pp. 18-20) that the primary welding occurred around the bond perimeter, and only secondary welding occurred in the center region. With the low-power, long-time schedule, it appears that, in addition to the improved cosmetic appearance, the way the metallurgical weld forms is also altered. Primary welding occurs in the center region as well as around the perimeter as shown in the lift-off pattern in figure 12. The bond pair shown in figure 10, typical of those made with the low-power, long-time schedule, had a pull strength approximately 1.5 times that of the bond pair shown in figure 11, typical of those made with the high-power, short-time schedule. A low-power, long-time series was made both before and after each high-power, short-time series to ensure that there were no significant changes in the surface finish of the tool. None were observed.

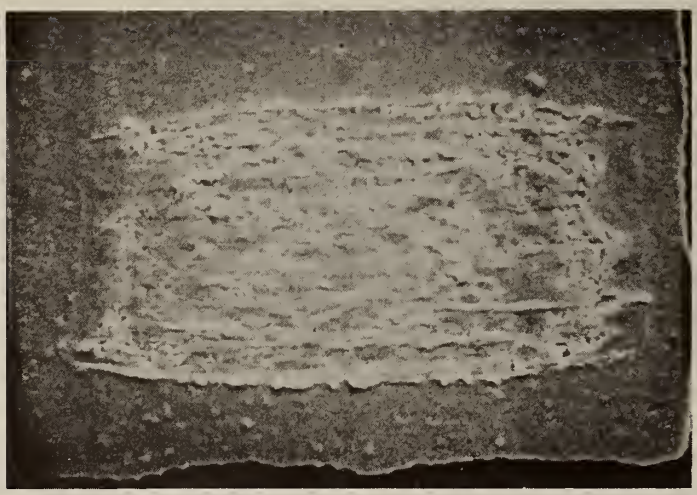


Figure 12. SEM photomicrograph of lift-off pattern of carefully removed adherent second bond made with the same low-power, long-time bonding cycle used for the bonds in figure 10 showing the uniform nature of the welding. (Magnification ∿750 X.)

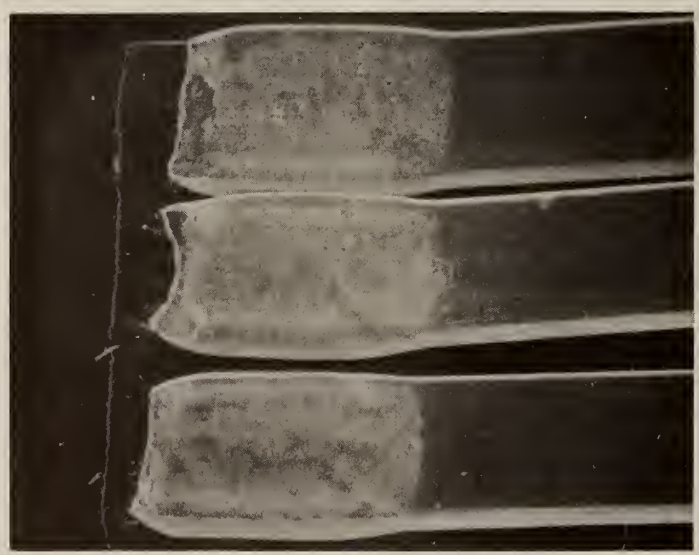


Figure 13. SEM photomicrograph of three bonds made with aluminum ribbon wire with cross-sectional dimensions 0.0005 by 0.0015 in. (13 by 38 μm) on a bonding pad 0.005-in. (127-μm) square. (The bonding schedule was low power [32-μin. (0.8-μm) peak-to-peak tooi tip amplitude] and medium time [80 ms]. Magnification ∿460 X.)

A test was conducted to establish that the positioning and deformation of the bonded ribbon wire could be controlled sufficiently to permit the use of the same size bonding pad that would be required for round wire of cross-sectional area equivalent to the ribbon wire. Three bonds were made with 0.0005 by 0.0015 in. (13 by 38 μm) aluminum (1% silicon) ribbon wire side-by-side on a bonding pad 0.005 by 0.005 in. (127 by 127 μm). The result, pictured in figure 13, should dispel any concern that larger bonding pads may be required if ribbon wire is used. The result is particularly significant in the case of high-frequency devices where the higher capacitance associated with larger bonding pads would degrade the high-frequency characteristics and in the case of overlay devices where sufficient area might not be available to accomodate larger bonding pads. (H. K. Kessler)

In-Process Bond Quality Determination — The basic concepts as well as the measurement system used for in-process bond quality studies have been described previously (NBS Tech. Notes 592, pp. 39-41, and 598, p. 27). The measurement system consists of a capacitor microphone, with a constricting taper, positioned so that it detects only the ultrasonic vibrations emitted from the bonding tool in the vicinity of a 60-kHz standing wave node. The resulting signal is displayed on an oscilloscope. During bonding the node shifts upward affecting both the amplitude and the harmonic content of the emitted vibrations. A characteristic oscilloscope pattern is observed for good bonds and assorted variations of this pattern are observed for weakly adhering bonds.

During this quarter, the measurement techniques and equipment were improved. A double-beam oscilloscope was employed so that the entire 50- to 100-ms bonding period can be displayed on the upper beam, while the waveform in any selected 200-μs portion is expanded and displayed simultaneously on the lower beam. A marker pulse indicating both the position in time and the width of the expanded portion is superimposed on the upper beam bonding signal. A simplified diagram of the apparatus is shown in figure 14. A typical oscilloscope pattern, obtained while making a normal bond with 0.001-in. (25-μm) diameter aluminum wire, is shown in figure 15. This bond was made with the usual constant-amplitude ultrasonic drive applied to the transducer.

Other experiments were carried out in which the amplitude of this drive was briefly increased by a factor of two to four for a short period during the normal bonding time. Figure 16a shows an oscilloscope trace of ultrasonic motion measured at the tip of the vibrating bonding tool rather than at a node. The phased burst of higher amplitude drive is clearly evident. Figure 16b gives the oscilloscope pattern from the node observed while a bond was made with the same bonding schedule as that used for the pattern shown in figure 15 except that a phased burst was added. Note that waveshape distortion is greatest during the burst period and that the envelope amplitude,

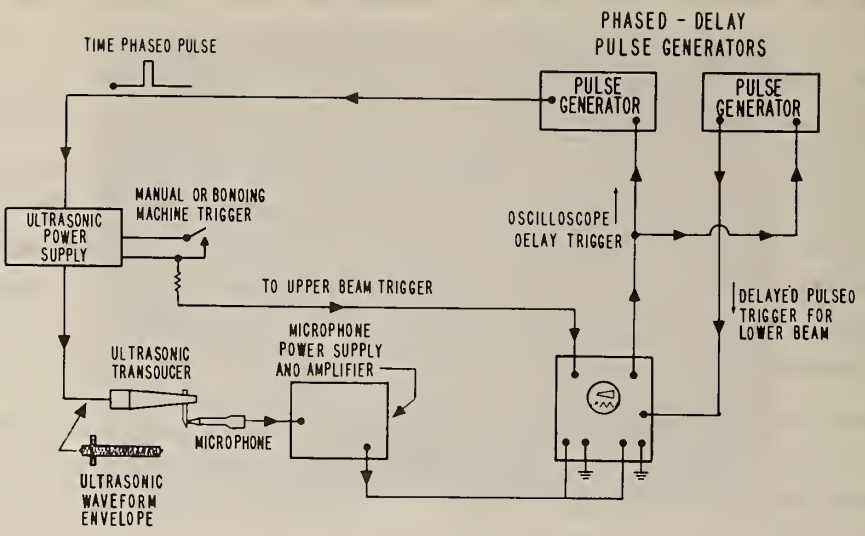


Figure 14. Simplified diagram of the pulse delay and phasing system used to monitor and study ultrasonic bonding.

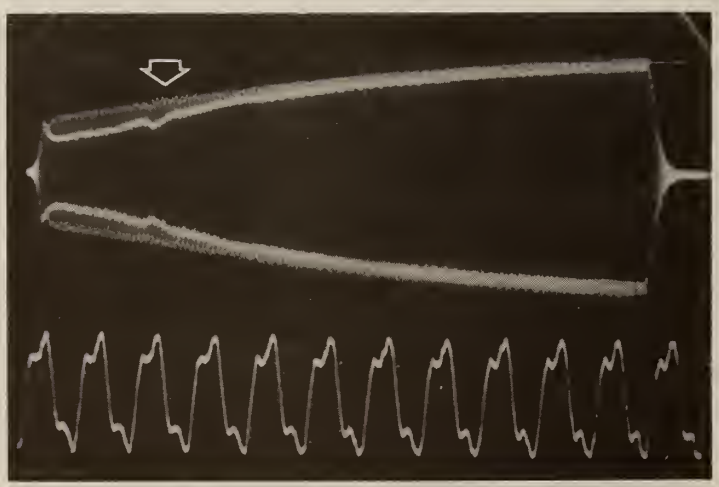
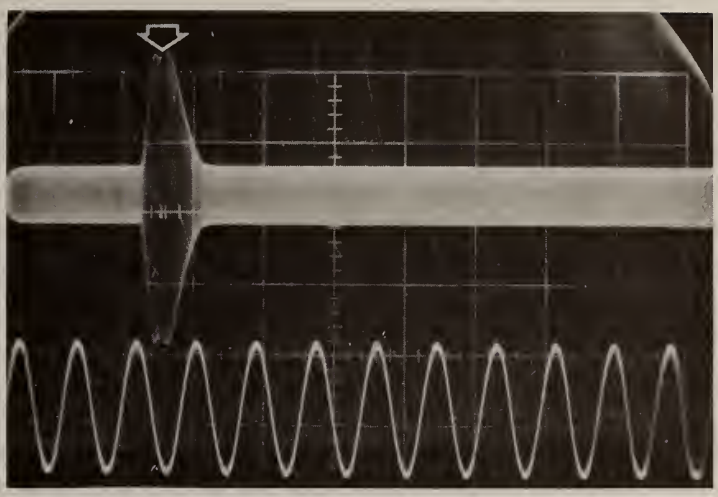
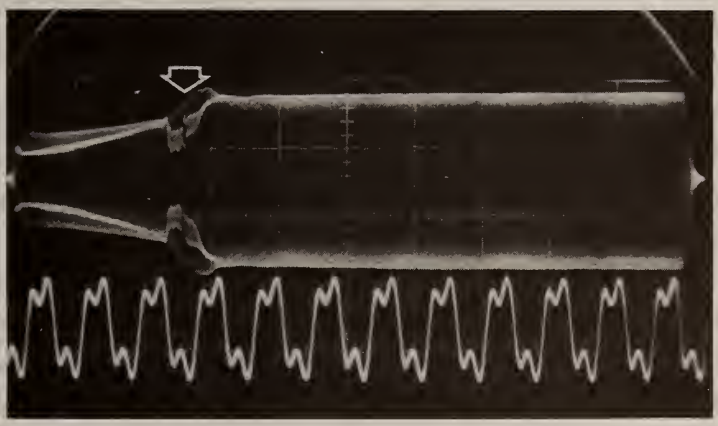


Figure 15. Bond formation pattern of a typical adherent bond. (The upper beam trace shows the entire bonding cycle. Horizontal scale: 5 ms/div. A portion of this trace indicated by the arrow is expanded on the lower beam trace. Horizontal sclae: 20 μs/div. Vertical scale for the lower trace is about 4/5 of that for the upper trace.)



a. The upper beam trace shows the ultrasonic vibration envelope of the motion of the bonding tool tip, demonstrating the amplitude variations in a phased burst bonding cycle Horizontal scale: 5 ms/div. The portion of this trace indicated by the arrow is expanded on the lower beam trace. Horizontal scale 20 μs/div. Vertical scale for the lower trace is about 1/2 that for the upper trace.



b. Bond formation pattern of a typical adherent bond made with a phased burst bonding cycle. The two traces are as described in figure 15 except that the vertical scale for the lower trace is about 2/3 that for the upper trace.

Figure 16. Oscilloscope displays of phased burst bonding cycle.

a monitor of the nodal shift and deformation, does not increase significantly after the burst. The bond, however, continues to become more adherent as determined by a shear test in which the tool (without ultrasonic excitation) is pushed against a portion of the bond. A study of such bond formation patterns has indicated that the burst resulted in the greatest increase in bond adherence when it was phased 10 to 15 ms after the initiation of a normal 50-ms bonding cycle. A typical burst is 2 to 5 ms long and is empirically adjusted in amplitude so that when it is added to the normal bonding amplitude it does not noticeably increase the bond deformation. The burst duration is adjusted so that the burst alone will not make a bond. These adjustments are not completely independent.

The phased burst appears to increase bond adherence without increased deformation or changed cosmetic appearance. However, this work has been performed as a laboratory experiment, and much more work needs to be done to prove that it is useful in a production environment. These experiments were performed with a single ultrasonic-power-supply, transducer combination because it was easily adaptable to phased-burst operation. Somewhat different oscilloscope displays were obtained when a different make of equipment was used. (G. G. Harman)

Mechanisms of Ultrasonic Bonding — In order to gain a better understanding of the mechanisms involved in ultrasonic wire bonding, experiments have been performed using some of the techniques developed at NBS, such as examination of bond lift-off patterns with the SEM and measurement of the bonding tool vibration amplitude with the capacitor microphone. While much of the work is subject to further experimental verification, some preliminary comments can be made. It appears that the tool transmits ultrasonic energy to the wire simply by moving back and forth over the top. It is not necessary for the tool to grip the wire and move it across the substrate metallization to make the bond. The shear force resulting from ultrasonic and pressure deformation of the wire appears to be a significant factor in the welding process. The roles of the various interfaces: tool-to-wire, wire-to-pad, pad-to-die, and die-to-package, seem to be of equal importance during the making of the bond. Preliminary results of this work have been reported [5]; a more complete report is being prepared [6].

(G. G. Harman and K. O. Leedy)

Pull Test Evaluation — To perform the wire-bond pull test, at least four variables must be considered: the rate of pull, the position of the hook along the span of the loop, the angle α with the normal to the line joining the bonds in the plane perpendicular to the plane of the bond loop, and the angle β with the normal to the line joining the bonds in the plane of the bond loop. It is necessary to know the sensitivity of the measured pull strength to each of these variables in order to determine how closely they must be specified in defining how to perform the pull test. It has

been determined previously (NBS Tech. Notes 560, pp. 30-31, and 592, p. 35) that over a reasonable range of rates, the pull rate had no effect on the resultant pull strength for single-level bonds. During this quarter, preliminary experiments were performed to evaluate the relative significance of two of the other variables. In all cases, the wire bonds tested were 0.001-in. (25-μm) diameter aluminum (1% silicon) wire ultrasonically bonded to aluminum pads. These single-level bonds had a bond-to-bond spacing of approximately 0.040 in. (1 mm) and a loop height of approximately 0.012 in. (0.3 mm). The principal mode of failure was breakage at the heel of the bond. In all experiments, ten bonds were tested at each value of the variable to assure that the results would be statistically meaningful.* All the bonds for each experiment were made during one run by one operator on one large substrate which contained many bonding pads.

Three experiments were performed to demonstrate the effect of the position of the pulling hook on the measured pull strength of an ultrasonic bond pair. The first of these three experiments involved pulling on the wire at various positions between the first and second bonds. The second and third experiments were similar in nature except that either the first or the second bond was prevented from breaking by the application of an epoxy adhesive.

The results of the first experiment are shown in figure 17 in which the measured pull strength of the bond pair is plotted against the position of the hook along the span of wire. The plotted points are the mean pull strength and the error bars represent the 95-percent confidence intervals for the mean. As might be expected, when the wire is pulled on the side nearest the first bond, it is this bond that breaks. Conversely, the second bond breaks when the force is applied nearest to it. A transition point, where the probability for either bond to break is nearly the same, occurs at the maximum value of measured pull strength. In the present case this point is found to be displaced more toward the second bond, as might be expected since the bonding machine used in these tests yields a stronger second bond than first.

The results of the second experiment are shown in figure 18. In this experiment, the effect of the second bond on the yield strength of the bond pair was eliminated by the application of epoxy to that bond. In this manner, only the strength of the first bond was tested at the different pulling positions. The three curves show the

* The selection is based on statistical considerations regarding the estimation of the mean of a population from a single sample (see Natrella, M. G., *Experimental Statistics*, NBS Handbook 91, August 1, 1963, p. 2-10). In some cases, failure in some of the tests occurred at a point other than the heel of the bond. The results of these tests were excluded from the averaging. All data reported represent the average of five or more tests. In cases where fewer than five bonds failed at the heel, no data are reported.

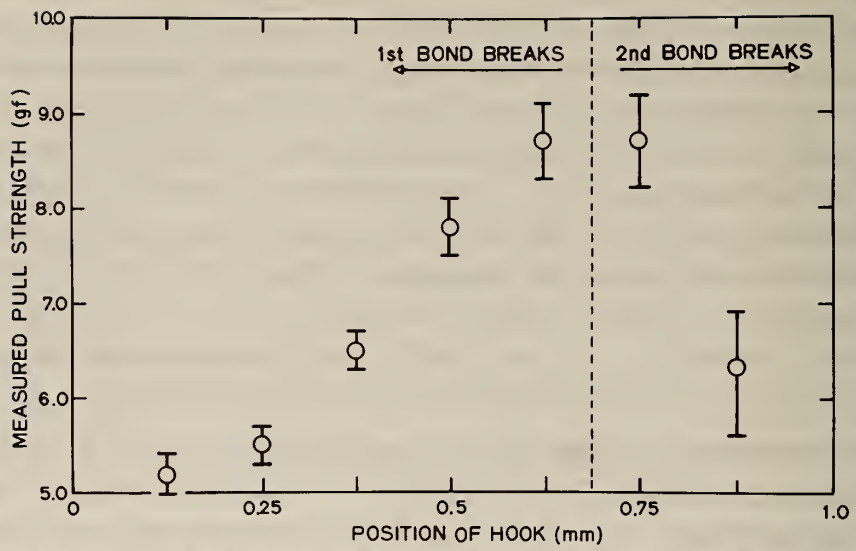


Figure 17. Measured pull strength of single-level bond pairs for different hook positions. (The first bond is at 0 and the second bond is at 1 mm).

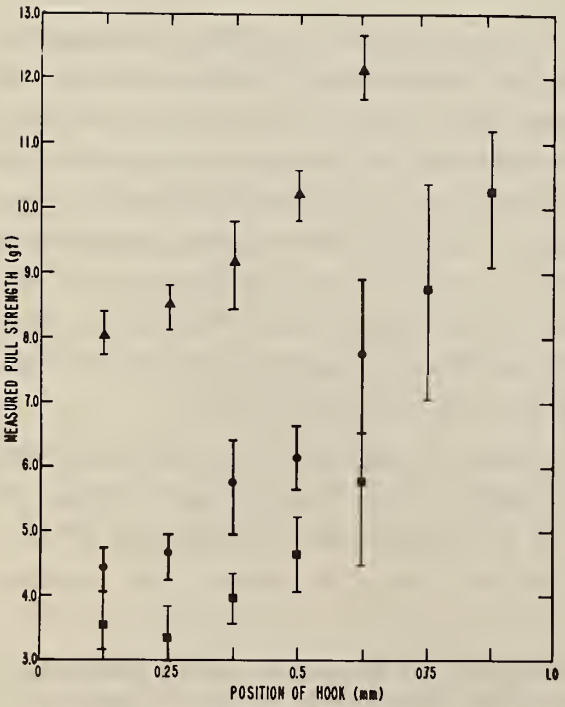


Figure 18. Measured pull strength of undeformed (▲), moderately deformed (●), and excessively deformed (■) single-level first bonds for different hook positions.

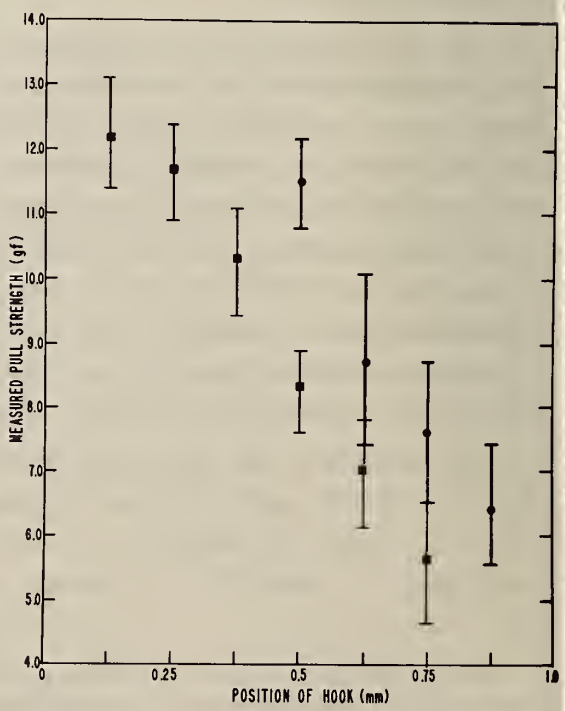


Figure 19. Measured pull strength of moderately deformed (●) and excessively deformed (■) single-level second bonds for different hook positions.

measured pull strength of bonds made at different ultrasonic power settings. The top curve is for a low power input to the bonding tool; the resulting bonds had a relatively undeformed heel. The middle curve is for intermediate power input; the resulting bonds had a much greater but not excessive deformation. The bottom curve is for high power input; the resulting bonds had the greatest deformation. That the shapes of the curves are roughly similar suggests that, although a reduction in bond strength occurs as the heel thickness decreases, heel deformation does not influence the variation of measured pull strength for the different positions along the bond loop.

The results of the third experiment, shown in figure 19, are very similar to those obtained for the second, being roughly a reflection of the results in figure 18. In this experiment the measured pull strength of the second bond was tested, epoxy being applied to the first bond. Results reported are for bonds made with intermediate and high power input. Second bonds made with low power input did not fail at the heel of the bond.

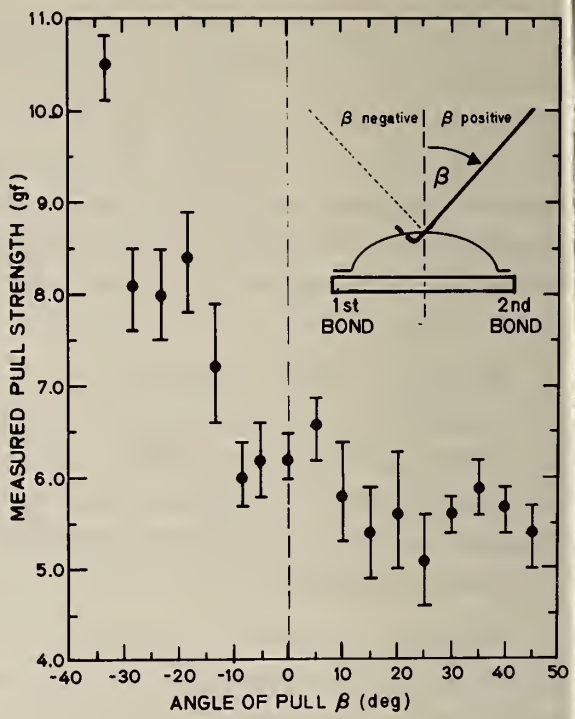
As might be expected, the results of these experiments indicate that the measured pull strength is very sensitive to the location of the placement of the hook during the pull test. For example, referring to figure 17, it is evident that placing the hook 0.005 in. (0.13 mm) from the midpoint of the loop results in a pull strength which is approximately 15 percent different than the pull strength obtained if the hook is positioned at the midpoint. If the error in the hook placement is halved, the apparent error in the pull strength is also halved.

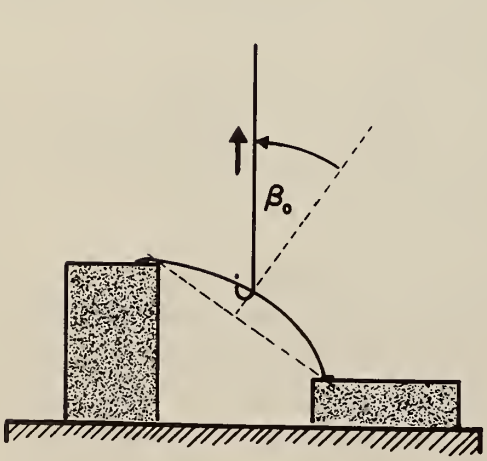
The dependence of measured pull strength on the angle β in the plane of the bond loop was also investigated. For a single-level bond pair, the accepted procedure for pulling a bond consists of the application of stress in a direction normal to the surface of the substrate. In this case the angle β is zero.

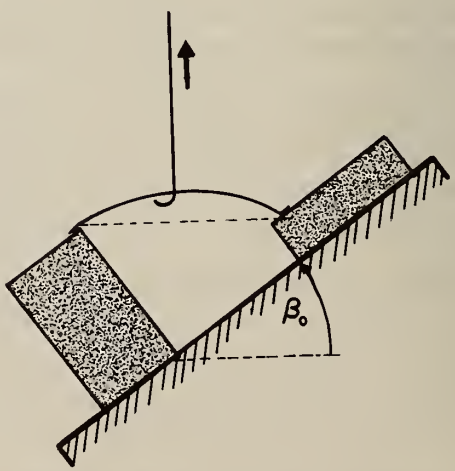
Bond loops were pulled at the midpoint of the loop at angles between 0 and 45 deg in both directions. The results are shown in figure 20. The mean values of the measured pull strength are denoted by the plotted points and the error bars represent the 95-percent confidence intervals for the mean. A curve of this type is to be expected since the second bond is stronger than the first. When the larger component of the force is applied to the first bond, the measured pull strength is lower and when the larger component of the force is applied to the second bond, the measured pull strength is higher.

The results for the larger values of β have yielded some insight into the pull test for two-level bond pairs. For a two-level bonding system, there are two ways the bond loop may be positioned for pulling as shown in figure 21. First, the substrate or package may be held level, which places each of the bonds at different

Figure 20. Measured pull strength of single-level bond pairs as a function of the angle of pull in the plane of the bond loop. (The inset shows the relationship of the angle of pull to the normal to the line joining the bonds. Note that the angle is positive when the pull force is inclined toward the second bond and negative when the pull force is inclined toward the first bond.)







a. Level substrate; nominal pull angle $\beta = \beta_0$. b. Tipped substrate; nominal pull angle $\beta = 0$.

Figure 21. Pull configurations for two-level bonds. (The direction of pull is indicated by the arrow.)

heights, and the force applied in a direction normal to the substrate. Alternatively, the substrate may be tipped to bring both bonds to the same vertical height; the configuration produced is more nearly similar to a single-level bond case, and the force is applied in a direction normal to an imaginary line joining the two bonds. The configuration in the level-substrate case is similar to that of a single-level bond system where the pulling is done at some angle β_0. It is apparent that tipping or not in the two-level bond system is essentially equivalent to varying the angle β. Although this comparison of single-level and two-level bond systems is in terms of bond-loop geometry only, one would expect that the general results shown in figure 21 would be applicable to the two-level system. That is, if the angle of pull is inclined toward the second bond (applying the larger component of force to the first bond) the measured pull strength is less than if the angle of pull is inclined toward in such the first bond (applying the larger component of force to the second bond). However, it should be noted that this analogy does not take into consideration the effects of the angles of the wire at the bond heels for the two situations. These effects can only be evaluated by experimental tests on two-level bond pairs.

(K. O. Leedy and C. A. Main)

Standardization Activities — Two preliminary investigations were conducted to obtain information on items under consideration in the Interconnection Bonding Section of ASTM Committee F-1 on Electronics. The first involved the question of wear of ultrasonic bonding tools. Eight tools, some alloy-tipped and some tungsten-carbide, supplied by several device manufacturers, were examined with the scanning electron microscope. One of the tools was new; the others had been used for different lengths of time. No evidence of wear was found in the used tools. However, no infomation regarding the number of bonds made with the tools was supplied, so conclusions relating tool wear to this quantity can not be drawn.

The second investigation addressed the question of possible differences in measured wire tensile breaking strength as determined by a standard tensile test [7] on 10-in. (254-mm) lengths of wire and as determined on specimens with length 1 to 2 percent of this value. A spool of wire was supplied by a wire manufacturer who tested it according to the usual procedure and reported a tensile strength of 17.7 gf (174 mN). The average tensile strength of 32 specimens 2.5 to 5 mm long, measured on the NBS pull test apparatus with the hot-melt glue puller (NBS Tech. Note 488, pp. 22-24), was about 10 percent lower than the value reported by the manufacturer. Although this result is consistent with previous comparisons between manufacturer's specifications and test results obtained here, more comprehensive experiments would be needed if it is desired to establish that the observed differences result from the differences in test methods.

(K. O. Leedy)

Bibliography and Critical Review — The bibliography of the open literature has been published [8] and is available on request. This bibliography contains more than 245 entries related to the testing, fabrication, and degradation of wire bonds. A comprehensive list of key words is used to describe the subject matter in each entry and the bibliographic list is indexed according to author and subject matter.

The critical survey paper is still undergoing editorial review. The preparation of an annotated bibliography of limited distribution reports has continued. About 75 reports have been selected and are being assigned key words and given annotations.

(H. A. Schafft)

Plans: Evaluation of ribbon wire for ultrasonic bonding will continue. A new wire clamp will be obtained and fitted to an existing round wire bonding machine that has a reproducible variable loop height adjustment as well as a bond tail length adjustment. Control of the loop height (not possible on the presently used machine) will permit good statistical bond pull strength data to be obtained, since the actual measured value obtained from this test is dependent upon the resolution of forces in the wire loop. Theoretical and experimental work on in-process studies of ultrasonic bonding tool motion will be continued in an effort to better understand and control bonding. Experimental and statistical analysis of significant factors in the wire bond pull test will continue. Editorial review procedures for the critical survey paper will be completed and the preparation of the text for printing will be initiated. The draft of the bibliography of limited distribution reports will be completed.

4.3. REFERENCES

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5. SEMICONDUCTOR DEVICES

5.1. THERMAL PROPERTIES OF DEVICES

Objective: To evaluate and improve electrical measurement techniques for determining the thermal characteristics of semiconductor devices.

Progress: Investigations were continued of the measurement of thermal resistance to compare the use of the collector-base voltage as the temperature sensitive parameter with the use of the emitter-base voltage. It was established that to compare measured values of transistor thermal resistance it is imperative to use the same temperature sensitive parameter, delay time, and measuring current, but further work is needed to determine the origins of the dependence of the measured thermal resistance on these quantities. Studies of the use of d-c current gain as an indicator for the formation of hot-spots due to current constrictions were extended to higher current levels.

Standardization Activities — Participation continued in the standardization activities of the following EIA-JEDEC committees involved in various aspects of standardization of semiconductor device thermal characterization: Committees JC-11 on Mechanical Standardization, JC-22 on Rectifier Diodes and Thyristors, JC-20 on Signal Diodes, JC-25 on Power Transistors, and JC-30 on Hybrid Integrated Circuits.

The devices for the preliminary round robin on thermal resistance being conducted in cooperation with Committee JC-25 are still in the hands of the third participant. Work was initiated on revising portions of a document on power transistors dealing with thermal characteristics that was recently letter balloted in Committee JC-25. Collection of information on test fixtures and test methods for characterizing thermal properties of microelectronic packages was continued in cooperation with Task Group JC-11.3-1 of Committee JC-11.

(F. F. Oettinger and S. Rubin)

Thermal Resistance Methods — Comparison of the collector-base voltage, V_{CB}, and the emitter-base voltage, V_{EB}, as the temperature sensitive parameter (TSP) to measure junction-to-case thermal resistance, $R_{\theta JC}$, was continued. Measurements of $R_{\theta JC}$ were made on two triple-diffused transistors, a double-diffused epitaxial transistor, a diffused-emitter epitaxial-base transistor and a single-diffused wide-base transistor that had power ratings in the range 20 to 35 W. Previously described test circuitry (NBS Tech. Notes 702, pp. 23-24, and 717, pp. 31-32) was used.

For the devices measured, it was found that for all values of the delay time, t_{meas}, between the end of the power pulse and the measurement in the range 10 to

100 μs the thermal resistance was up to 10 percent smaller when V_{CB} was used as the TSP than when V_{EB} was used. For the triple-diffused and epitaxial transistors the percent difference decreased as t_{meas} was increased from 10 to 100 μs. There was no appreciable change in the measured $R_{\theta JC}$ of the single-diffused wide-base transistor for t_{meas} in the range 10 to 100 μs; the difference between $R_{\theta JC}$ measured with V_{EB} as the TSP and with V_{CB} as the TSP was consistently smaller for this type of device than for the other types of devices.

Measurements made on a triple-diffused transistor to study the dependence of the measured $R_{\theta JC}$ on source voltage, source impedance, and magnitude of the measuring current for both V_{EB} and V_{CB} as the TSP indicated that the controlling factor was the magnitude of the measuring current. Subsequent measurements made on both a triple-diffused transistor and a single-diffused wide-base transistor indicated that for measuring current ranging from 6.5 to 22.5 mA the measured $R_{\theta JC}$ generally decreased as the measuring current was increased. The extent of the change was dependent both on the TSP and the device geometry.

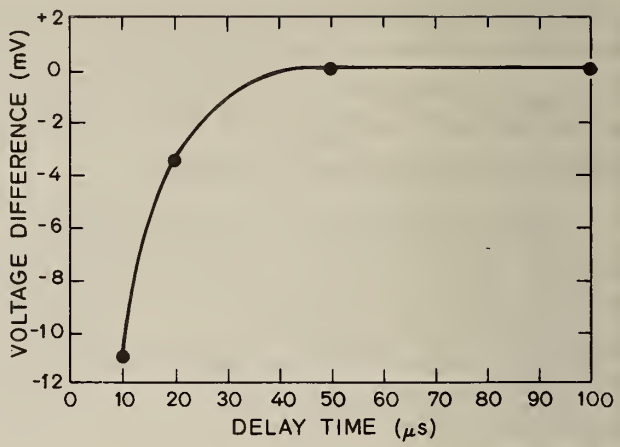
It is therefore evident that when comparing measured values of transistor thermal resistance the same temperature sensitive parameter, delay time, and measuring current must be used unless it has been demonstrated for the particular type of device being measured that any different measuring conditions used lead to equivalent results. Further work is needed to determine why variations in these conditions cause the observed changes in measured $R_{\theta JC}$. (S. Rubin and F. F. Oettinger)

A calculation was performed to determine what temperature is measured when the forward voltage of a diode is used as the temperature sensitive parameter if an arbitrary temperature distribution exists across the diode junction area. For the calculation it was assumed that the current was one-dimensional, perpendicular to the plane of the junction, and that the low level constant measuring current produced no additional internal heating of the diode. The results of the calculation were that the temperature, T, indicated by the forward voltage was the weighted average temperature:

$$T = \frac{\sum_i A_i T_i}{\sum_i A_i},$$

where T_i is the temperature of the element of area A_i. The indicated temperature is therefore only a fraction of the peak junction temperature. In reality, only a small class of devices have one-dimensional current. For devices with terminals either on the same surface or on perpendicular surfaces of the chip, current in two or more directions must be considered. In some cases, part of the junction may be de-biased by lateral current. For devices in which junction de-biasing occurs, the measured

Figure 22. Difference between the value of the base-emitter voltage extrapolated to zero power and the d-c calibration value for a triple-diffused silicon power transistor. (The temperature coefficient of the base-emitter voltage is -2.07 mV/°C. The base-emitter d-c calibration voltage was 626 mV for a measuring base current of 6.5 mA. Case temperature was held at 25°C.)



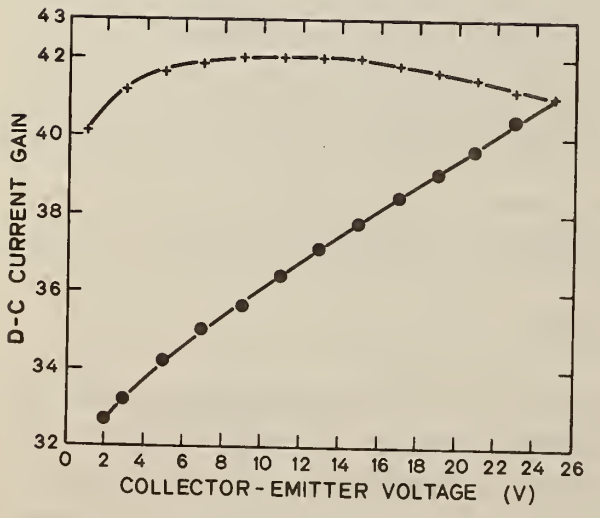


Figure 23. Common emitter current gain as a function of collector emitter voltage for a single-diffused, wide-base silicon power transistor. (The collector current was held constant at 1 A. For the upper curve (+) the case temperature was held constant at 25°C. For the lower curve (●) the peak junction temperature was held constant at about 94°C.)

temperature is probably a different fraction of the peak junction temperature than this equation would indicate. (D. L. Blackburn)

An investigation was begun to understand the origin of the frequently occurring difference between the straight-line extrapolation to zero-power of the measured value of the TSP as a function of power and the d-c calibration value at the zero-power level (NBS Tech. Note 598, pp. 30-33). If this difference can be eliminated, the procedure for measuring $R_{\theta JC}$ can be simplified by eliminating one of the two measurements of the TSP now required for the calculation of thermal resistance. To illustrate the problem, the extrapolated and calibration values of the TSP, V_{EB}, measured previously (NBS Tech. Note 598, p. 32) on a 35-W, triple-diffused silicon transistor are shown in figure 22 for various values of delay time, t_{meas}. It can be seen that the maximum deviation of 10 mV occurs at the shortest value of t_{meas} investigated and that the deviation decreases as t_{meas} is increased.

Additional measurements were made on both triple-diffused and single-diffused silicon power transistors with both V_{EB} and V_{CB} as the TSP. For the triple-diffused transistor, the extrapolated values for t_{meas} = 10 μs, for both V_{CB} and V_{EB}, were found to be approximately 10 mV below the d-c calibration value. For the single-diffused wide-base device, the 10-μs intercept was 5 mV below the d-c calibration value for V_{EB}, but only 1 mV below for V_{CB}. In all cases, the extrapolated value increased with longer delay times and was essentially the same as the d-c calibration value for t_{meas} = 50 μs. Varying the measuring current from 6.5 to 22.5 mA had no significant effect on the magnitude of the difference observed for any case.

Thermal resistance measurements were also made on one of the diodes used in the die attachment evaluation study to determine whether a similar difference existed. Measurements of $R_{\theta JC}$ as a function of power were made for delay times of 10, 50, and 100 μs on two different measuring circuits. In all cases, the straight-line, zero-power extrapolation converged to the d-c calibration value of the TSP. An experiment was then undertaken to measure the thermal resistance of a triple-diffused transistor connected as a diode in three separate configurations:

1. grounded collector, with emitter connected to collector,
2. grounded collector, with emitter connected to base, and
3. grounded emitter, with collector connected to base.

In configuration 1, the initial transient was very long and measurements could not be made until the delay time exceeded 20 μs. In configurations 2 and 3, measurements could be made with the delay time as short as 10 μs, but the computed thermal resistance was significantly higher than that computed from measurements made with the device connected as a transistor. Even though the measured $R_{\theta JC}$ was higher when

operating the transistor in the diode connections, the straight-line extrapolation for the various delay times converged to the d-c calibration value of the TSP at zero power.

It is still not clear whether the discrepancy, which occurs when transistors connected in the normal way are measured, is dependent on the transistor under test or whether there is an interaction between the transistor and the test circuit.

(S. Rubin, F. F. Oettinger, and R. L. Gladhill)

Screen for Hot Spots — The use of d-c common-emitter current gain, h_{FE}, as an indicator for the formation of hot spots due to current constrictions in power transistors has been discussed previously (NBS Tech. Note 702, pp. 25-26). In this technique, the collector current and case temperature are held constant. Hot-spot formation is indicated by a distinct decrease in h_{FE} with increasing collector-emitter voltage, V_{CE}.

Further studies were initiated to evaluate the usefulness of the h_{FE} measurement for the detection of hot spots at high collector currents. Measurements of h_{FE} as a function of collector voltage were made on a single-diffused, wide-base, 25-W power transistor for collector currents up to 2 A. The device was coated with a thermographic phosphor to permit visual observation of hot spots and to permit estimates of the surface temperature to be made. The device selected for the initial measurements was not subject to hot spots at low collector currents and so was not expected to be susceptible to them at high currents. As shown in figure 23, for constant case temperature and a collector current of 1 A, h_{FE} begins to decrease with V_{CE} beyond a certain value, although no current constrictions (as indicated by elevated temperature in localized regions) were observed visually. Typical characteristic curves published by the manufacturer of the device indicate that, for fixed V_{CE}, the temperature coefficient of h_{FE} reverses from positive to negative beyond a certain collector current. Therefore, above a certain collector current level, h_{FE} decreases with increasing junction temperature.

To determine if the measured decrease in h_{FE} with V_{CE} was a result of an increase in junction temperature for collector currents at 1 A and above, measurements of h_{FE} were made as a function of V_{CE} while the junction temperature was kept constant by varying the transistor case temperature so as to maintain a constant peak surface temperature on the chip as indicated by the light output of the phosphor. As shown in figure 23, at a collector current of 1 A, h_{FE} continued to increase with increasing V_{CE} to the maximum applied voltage. Thus, it was concluded that the decrease in h_{FE} at high collector currents was due to the increase in junction temperature.

This limitation does not significantly detract from the use of h_{FE} as a technique to detect hot-spots due to current constrictions since it is under low-current, high-voltage operating conditions that severe hot spots are most likely to form due to current crowding. (F. F. Oettinger and D. L. Blackburn)

Plans: Work on standardization activities related to thermal measurements will continue. The literature search and work on the bibliography on thermal measurements of semiconductor devices will be continued. Studies will continue to determine why the TSP measured on transistors as a function of power does not extrapolate linearly to a zero-power value equal to the d-c calibration value. Since a number of industrial users of semiconductor devices measure thermal resistance of transistors in diode operating modes, study will continue of these modes as compared with the transistor operating mode. Further measurements of h_{FE}, especially at high current levels, will be made on a variety of device types. The results of the study of the use of current gain as an indicator for the formation of hot spots due to current crowding in power transistors will be summarized [1].

5.2. MICROWAVE DEVICE MEASUREMENTS

Objective: To study the problems and uncertainties associated with the measurement of microwave devices, and to improve the techniques of these measurements.

Progress: Clamping of the waveguide system has been completed. Preliminary tests indicate that this clamping successfully reduces power changes during measurement runs due to mechanical forces such as ejection from the mixer of the diode under test. Measurements to ascertain conversion loss repeatability before and after clamping were taken, but have not been evaluated as yet. It has been noted, however, that forces on the mixer (holder) far in excess of those required for diode ejection do not change the output voltage by more than 0.1 mV, as opposed to the several millivolt changes that could previously be obtained with similar forces. To add further stability, a rigid table to support the system, formed from welded aluminum L-beams topped with a 1-in. (2.54-cm) thick aluminum slab, was obtained.

(J. M. Kenney, L. M. Smith, and F. R. Kelly)

The third micrometer-head stop was installed on a hinged platform on the rotary-vane attenuator which had been modified to serve both as a modulator and as a modulation standard. Based on the results of a calibration described below, the design of the hinged platform appears to be quite satisfactory. Good resetability of the platform was achieved by use of orthogonal pins and grooves for location, the hinge being loosely fitting. (J. M. Kenney and L. M. Smith)

This attenuator was hand-carried to the NBS Boulder Laboratories for a calibration* that consisted of (1) setting the zero stop for minimum insertion loss, (2) setting the recently added stop, which is mounted on the hinged platform, to add a loss of 0.486 dB, and (3) after swinging this stop clear, setting the remaining stop to add a loss of 1.000 dB to the zero position loss. After the stops were set and locked, the loss increments were measured a number of times to obtain repeatability data. The repeatability of the 0.486-dB increment was reported as ±0.0014 dB (three standard deviations) and that of the 1.000-dB increment as ±0.0019 dB (three standard deviations). In addition to these repeatability uncertainties, it was reported that a conservative systematic error uncertainty of ±0.005 dB was assigned to the calibration. The system on which the calibration was made is still undergoing evaluation, and this systematic error uncertainty is expected to be reduced.

The 0.486-dB increment was selected because it is the peak-to-carrier ratio for a 5.749 percent linear modulation that results in a peak-to-trough ratio of exactly 1 dB. By setting the local oscillator power (with a mounted bolometer in place of the mixer) when the attenuator is set at the 0.486-dB stop on the hinged platform, the peak or trough power levels that would be reached by linear modulation can be obtained by rotating the attenuator vane to, respectively, the zero stop (+0.486 dB power change) or the 1.000-dB stop (-0.514 dB power change). Mixer conversion (insertion) loss is obtained from the resulting values of output voltage at the mixer i-f port, with the use of an equation derived from an assumption of linear sinusoidal modulation with the same peak and trough values as the experimental incremental ones.

In order to obtain distinct d-c (self-bias) and a-c (i-f) loads as specified, a 100-Ω resistor and a 300-Ω resistor are connected in series across the i-f terminals. The sum of these resistors is the specified a-c load for a type 1N23 diode. The 300-Ω resistor is grounded at one end and is connected in parallel with a constant current generator whose output is used to null the voltage across it while the r-f power is unmodulated. This nulling procedure in effect short circuits the 300-Ω resistor, leaving only the 100-Ω resistor to correctly self-bias the diode. When the r-f power is modulated, the change in output current must pass through both load resistors, thus giving the correct a-c load. If the mixer were perfectly linear, and if the modulation were linear and sinusoidal (or of any other antisymmetrical waveform), then the average of the output currents at the peak and at the trough of the modulation cycle, or for any other pair of points 180 deg apart, would be the same as the unmodulated output current;

* The attenuator was calibrated by W. Larson and R. Hunter of the NBS Electromagnetics Division. At the same time, five mounted bolometers and two dry calorimeters were calibrated by M. Weidman of the Electromagnetics Division.

the true d-c level of the output would therefore be unchanged by the modulation. A modulation asymmetry that results in a change of the d-c output is equivalent to an error in local oscillator (carrier) power and therefore in signal (sideband) power. Although reducing the modulation percentage tends to reduce errors due to modulation asymmetry as well as to mixer nonlinearity, it also tends to increase errors in setting the modulation and reading the output; it is thus always preferable to maintain a symmetrical modulating waveform, as is being done by use of the three-stop attenuator with the 0.486-dB and 1.000-dB increments.

The first meeting of the microwave mixer and detector task group of the IEEE-GED Standards Committee for Electron Devices was held at NBS on October 14. The topic for discussion was IEC document 47(Central Office) 376, a standard for mixer diode measurement methods. An extensive and detailed review of the standard was prepared and distributed to all task group members for comment. Substantial deficiencies in the IEC document were noted, and a recommendation was made that the U.S. National Committee oppose its adoption. A detailed list of technical criticisms and proposed changes accompanied this recommendation.

Comments on proposed changes of definitions and symbols for microwave diodes in MIL-S-19500, General Specification for Semiconductor Devices, and suggestions for other changes, were made to the appropriate military agencies early in December. Among the newly suggested changes which may be of general mixer measurement interest is the redefinition of conversion loss to allow its calculation using delivered as well as available output power, as has been done with noise figure. It was also suggested that symbols and terminology be modified to distinguish between standard and measured i-f average noise figure and between standard and measured overall average noise figure.

(J. M. Kenney)

Plans: The mixer output circuit used for the incremental modulation measurements will be rebuilt to permit the direct measurement of output conductance and matched-load voltage (NBS Tech. Note 592, pp. 57-58). A new low-drift op-amp will be installed in the leveling loop to increase the stability of the local oscillator power level. The waveguide system will be placed on the new all-metal bench, which will be modified by the addition of an overhead equipment shelf and shock-mounted casters.

5.3. CARRIER TRANSPORT IN JUNCTION DEVICES

Objective: To improve methods of measurement for charge carrier transport and related properties of junction semiconductor devices.

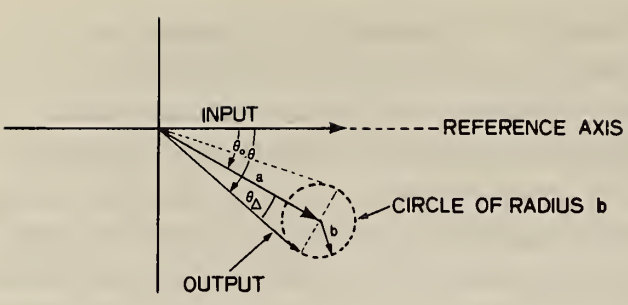


Figure 24. Vector diagram showing input-signal, transistor transfer function (a), extraneous error signal (b) and output signal for a phase-delay measurement system.

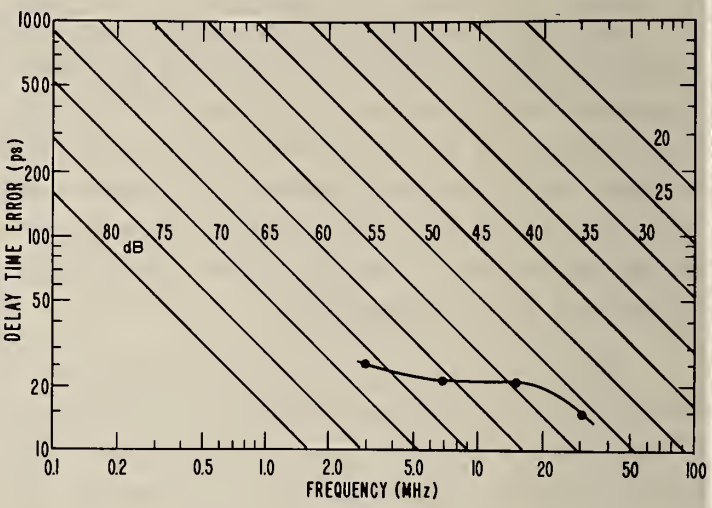


Figure 25. Maximum phase delay error due to extraneous coupling as a function of measurement frequency and isolation ratio. (The plotted curve shows the results of inter-channel isolation measurements on the Sandia bridge constructed at NBS.)

Figure 26. Photomicrograph of typical R-C plug-in network assembled on a TO-5 header. (Magnification ~8.4 x).

Progress: A general explanation was developed to account for the previously reported significant differences in delay time as measured on different instruments or on the same instrument at different frequencies. Six R-C plug-in networks with time constants in the range 212 to 700 ps were fabricated for use in experiments to test this explanation and to characterize delay-time instruments. Delay-time measurements were made with a Sandia bridge on several transistors and compared with measurements performed on the same transistors by another laboratory with a similar test system. S-parameter measurements were made on a type 2N2219 transistor; the base transit time obtained from an analysis of these measurements showed substantial agreement with the results of earlier measurements made with a vector-voltmeter test system. An analysis was completed to determine the delay-time error introduced into the vector-voltmeter test system by capacitive or inductive components in the test circuit collector-base impedance.

Error Analysis and Determination — An analysis was completed that shows why extreme care must be taken in the design and construction of circuits for the measurement of transistor delay time. Many circuits that might otherwise be considered quite adequate for use at measurement frequencies in the megahertz range may give erroneous measurements of delay time. The effects are most severe for circuits designed to measure delay time of high-frequency transistors at 1 to 30 MHz, well below their design-maximum operating frequency.

The presence of an extraneous signal at the measurement frequency, that might result from a lack of adequate shielding between the signal generator and the detector or from undesirable internal coupling between various parts of the measurement circuit, can introduce error into the delay time. The origin of this error can be seen with the aid of figure 24. The vector of magnitude a at the angle θ_0 below the reference (input) axis represents the transfer function for the transistor, and the vector of magnitude b represents the extraneous signal at the measurement frequency. The effects are most severe when a and b are orthogonal; for this case, in which the output signal makes an angle θ_Δ with the desired signal a, $\tan \theta_\Delta = b/a$. For $\theta_\Delta \ll \pi/4$, b/a is approximately equal to θ_Δ and the corresponding error in the phase delay time (NBS Tech. Note 717, pp. 37-40) in picoseconds is

$$\tau_\Delta = (10^6/2\pi f)\ (b/a),$$

where f is the frequency in megahertz. If the ratio b/a expressed in decibels is represented as $-R$ the expression for the error in phase delay time becomes

$$\tau_\Delta = 10^6/[2\pi f\ \text{antilog}_{10}\ (R/20)].$$

The family of straight lines in figure 25 which relate τ_Δ to f for various isolation

ratios, R, can be used to determine graphically the maximum delay-time error from circuit isolation measurements. The curve plotted shows the results of interchannel isolation measurements in the frequency range 3 to 30 MHz made on the Sandia-type delay-time bridge constructed at NBS. Other bridges, constructed to essentially the same plans, may have different isolation characteristics.* These differences in isolation characteristics may contribute significantly to the differences in delay times measured on different instruments at the same frequency or on the same instrument at different frequencies. (D. E. Sawyer)

To attempt to verify the above calculation and quantify the differences between the characteristics of different instruments or of a given instrument at different frequencies, six resistance-capacitance networks of known time constants in the range 212 to 700 ps, and hence known delay times, were assembled on TO-5 headers for measurement in the instruments. Figure 26 is a photomicrograph of an assembly of this type. The circuit is a tee with two resistors of equal value R connected in series between the emitter and collector pins, and a capacitor of value C connected between the header and the junction of the resistors. The header is electrically connected to the base pin. The 0.001-in. (25-μm) diameter gold connecting wires are bonded ultrasonically to the components and pins, and the film resistors are spaced from the header with 0.1-in. (2.5-mm) high ceramic pillars to reduce the distributed capacitance between the resistors and the header.

If one assumes that the equivalent circuit of the instrument is known and that the network can be treated as a lumped circuit, one can predict the delay-time value which should be read with such a circuit in the transistor socket, and the difference, if any, between these values and the actual readings can be analyzed for a key to the real behavior of the instrument. If the measurement angular frequency, ω, is such that $\omega\tau_{RC} << 1$, where $\tau_{RC} = RC$, then the delay time as measured for these networks with the vector-voltmeter system is τ_{RC} if effects due to parasitics such as header capacitances can be neglected. For the idealized Sandia bridge, the predicted delay-time is $\tau_{RC}\,(R_z + R)/(R_z + 2R)$, where $R_z = 100\ \Omega$. Other types of delay-time instruments can be analyzed similarly to yield the delay times expected.

Comparative Delay-Time Measurements — Measurements of delay time in several types of high-frequency transistors were made with both the Sandia bridge and vector-voltmeter

* For example, W. H. Sullivan, Sandia Laboratories, has recently demonstrated (private communication) that it is possible to construct models of the Sandia bridge with interchannel isolation greater than 80 dB for all frequencies of interest. Under these conditions, maximum delay-time errors due to interchannel coupling are, for example, less than 2 ps at 10 MHz, and can be neglected.

circuit. As reported previously (NBS Tech. Note 717, pp. 36-37) there were differences in the results obtained on the two systems that were larger for some device types than for others. Typical results for a type 2N2219 transistor are shown in figure 27. In addition to the significant difference between systems, measurements with the Sandia bridge were highly dependent on frequency. The variations encountered in making repeated measurements at the same conditions are substantially less than the observed differences.

During the present quarter, delay-time measurements were made at NBS and at another laboratory, both using Sandia bridges, on two additional types of high-frequency transistors. Measurements at NBS were made over the frequency range 3 to 30 MHz; at the other laboratory, measurements were made only at 10 MHz. These results, shown in figure 28 show a much smaller dependence on frequency. In addition, the agreement between test systems is noticeably better for one device than for the other, although both are considered to be quite good for devices with such small delay times.

The two instruments have somewhat different socket arrangements. In each case the location of the pick-off point for the null detector was selected in such a way as to least affect the measurement. In the NBS measurements on the transistors reported above, it was found that with the pick-off point on the portion of the transistor collector lead (about 2.5-mm long) between the transistor can and the socket, the delay time was 25 ps shorter than the value measured with the pick-off point at the collector socket lug. Values reported were measured at the former point and are believed to represent better the delay time of the transistor because the inductive effects of the socket pin are minimized. (D. E. Sawyer)

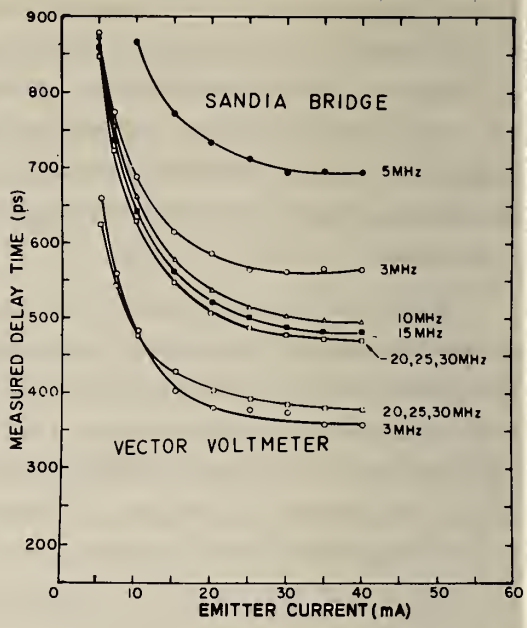
Base transit time can also be determined from S-parameter measurements; the method has been outlined in detail by K. R. Smith [1]. Both amplitude and phase of the four S-parameters are measured over a range of emitter biases and at several frequencies in the region in which h_{fe} is decreasing with frequency at a rate of 6 dB per octave, and the small-signal forward current gain, h_{fe}, is calculated from the S-parameters:

$$\overline{h_{fe}} = \frac{2\overline{S_{21}}}{(1 - \overline{S_{11}})\,(1 + \overline{S_{22}}) + (\overline{S_{12}}\;\overline{S_{21}})} \quad ,$$

where a bar over a term indicates a complex quantity.

Transition frequency, f_T, is determined from the h_{fe} measurements either by plotting log $|h_{fe}|$ against log frequency and determining the unity gain intercept on the frequency axis, or by multiplying $|h_{fe}|$ by the frequency at which the measurement was made if it is known that this frequency is in the range where h_{fe} is decreasing with frequency at a rate of 6 dB per octave. Total delay time, $\tau_T = 1/(2\pi f_T)$, is then

Figure 27. Delay time of a 2N2219 transistor measured on two systems of different types at frequencies from 3 to 30 MHz.



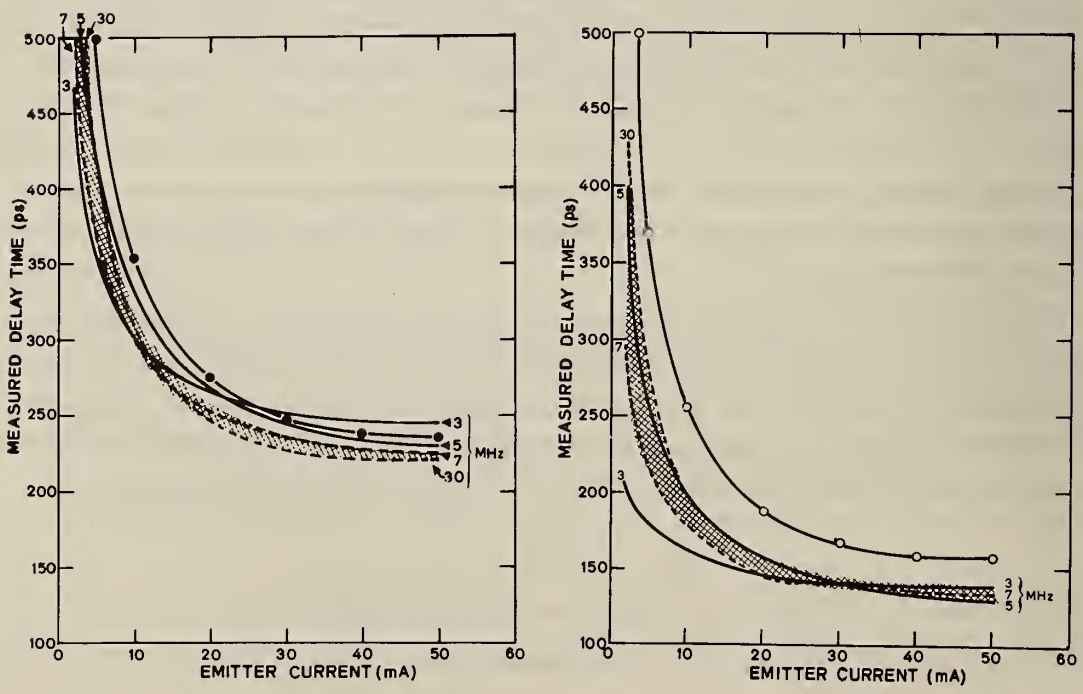


Figure 28. Delay time of two high-frequency transistors each measured on two different systems of the same type. (Measurements were made at frequencies from 3 to 30 MHz on one system at NBS. Measurements between 7 and 30 MHz were generally within the shaded area. Measurements were made only at 10 MHz on the other system at another laboratory: ●,○).

calculated and plotted against the reciprocal of emitter current as illustrated in figure 29. Where, as in the present case, the curve has a straight line portion, it can be extended to the total delay time axis. This intercept is customarily interpreted as the base transit time. The data plotted in the figure are for a type 2N2219 transistor operated under the same bias conditions as the transistors of the same type previously measured. The base transit time is essentially the same as that obtained from measurements made with the vector-voltmeter system (figure 27). (G. J. Rogers and F. R. Kelly)

Vector-Voltmeter Circuit Analysis — One problem with the vector-voltmeter circuit assembled as shown in figure 31 is that the connection between collector and base cannot be a true short because the a-c signal must be by-passed without interfering with the d-c bias of the transistor. An analysis has been carried out by procedures reported previously (NBS Tech. Note 717, pp. 37-40) to determine the effect of reactance in this circuit on the measurement of phase shift between the emitter and base currents of the transistor under test.

If the connection between collector and base is idealized as a short circuit (zero resistance and reactance), the phase delay time is given by:

$$\tau = \tau_\alpha + \tau_e - (\tau_c/h_{fe}),$$

where τ_α is the delay time associated with the transit of minority carriers across the base region and collector junction, τ_e is the emitter time constant, r_eC_e (r_e is the dynamic resistance of the forward-biased emitter junction and C_e is the transition-region capacitance of the base-emitter junction), τ_c is the collector time constant, r_bC_c (r_b is the base resistance and C_c is the transition-region capacitance of the base-emitter junction), and h_{fe} is the small-signal, common-emitter current gain.

If instead of a short circuit the connection is a capacitive reactance, which it is in practice when the by-pass capacitor retains its capacitive characeristics at the measurement frequency, the phase delay time is given by:

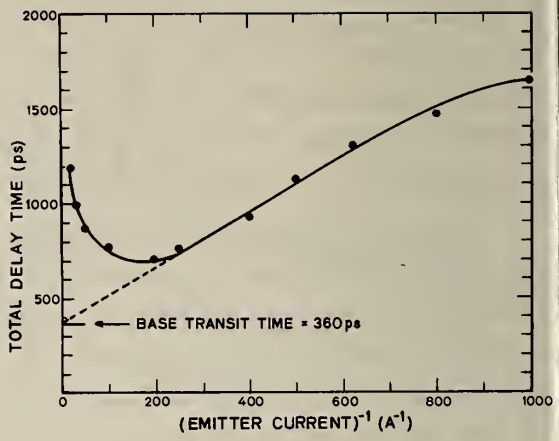
$$\tau = \tau_\alpha + \tau_e - \tau_c \{h_{fe}^{-1} + [1 + (C_s/C_c)]^{-1}\},$$

and a new quantity, $[1 + (C_s/C_c)]^{-1}$, appears in the last term, where C_s is the collector-to-base by-pass capacitor. The capacitive reactance has little effect on the phase delay time if $C_s >> C_c$.

If there is inductance in series with the by-pass capacitor (lead inductance, for example), the by-pass circuit may be series-resonant at an angular frequency lower than the measurement angular frequency, ω. The connection is then an inductance, L, at the measurement frequency, and the phase delay time is given by:

$$\tau = \tau_\alpha + \tau_e - \tau_c \{h_{fe}^{-1} + [1 - (\omega_0/\omega)^2]^{-1}\}$$

Figure 29. Transit time of a 2N2219 transistor derived from S-parameter measurements. (V_{CB} = 5V).



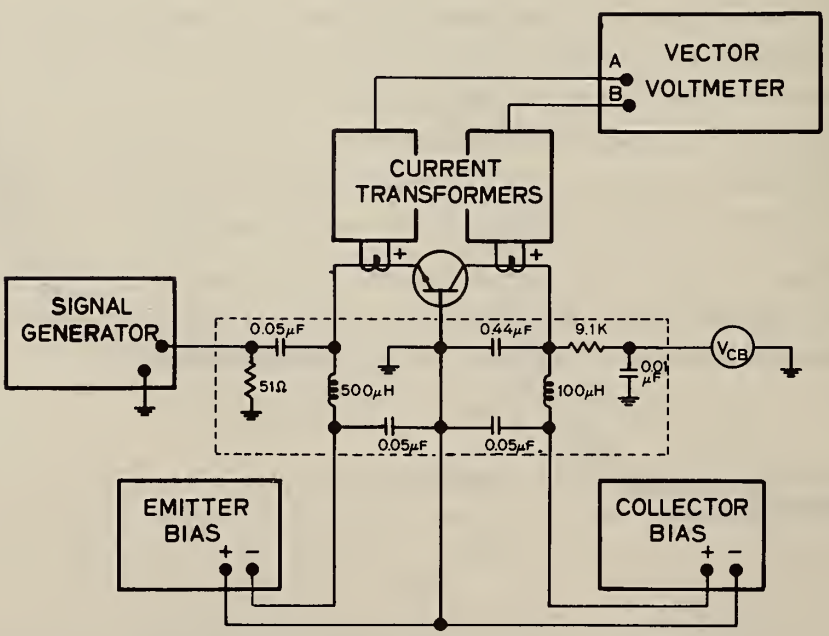


Figure 30. Vector-voltmeter delay-time measuring circuit.

where $\omega_0 = (LC_c)^{-1/2}$ is the angular frequency at which the inductance of the by-pass circuit resonates with the transition-region capacitance of the base-collector junction of the transistor under test. The added quantity, $[1 - (\omega_0/\omega)^2]^{-1}$, which appears in the last term, has little effect on the phase delay time if $\omega << \omega_0$. (G. J. Rogers)

Plans: Base-transit time measurements will be made by the S-parameter method on several transistor types and compared with the results of measurements made with the Sandia bridge. Preparations will be made for an interlaboratory comparison of S-parameter measurements. Measurements on the Sandia bridge using R-C plug-in networks will be analyzed in an effort to display the actual, rather than the idealized, equivalent circuit in an attempt to understand some of the effects observed when using the bridge. Continuing work will be focussed on exploring ways of localizing exact sources of errors, and on means of incorporating the associated correction factors into the equivalent circuits.

5.4. SILICON NUCLEAR RADIATION DETECTORS

Objective: To conduct a program of research, development, and device evaluation in the field of silicon nuclear radiation detectors with emphasis on the improvement of detector technology, and to provide consultation and specialized device fabrication services to the sponsor.

Progress: Further neutron irradiations were performed in order to gain additional information on the long-term stability of lithium-drifted and surface-barrier silicon nuclear radiation detectors. The ambient exposure test study was completed.

Radiation Damage — Previous experiments (NBS Tech. Note 702, p. 33) showed that irradiation of lithium-drifted silicon [Si(Li)] detectors with neutrons at fluences of about 6×10^{10} cm^{-2} caused degradation of detector characteristics which persisted after irradiation. Annealing effects were not noted during two weeks of observation; charge collection efficiency was observed to deteriorate, however, starting about three weeks after irradiation. In order to determine the maximum neutron fluence that detectors can tolerate from the neutron output of a radioisotope thermoelectric generator in a deep space flight experiment, additional experiments were carried out.

Three 2-mm thick Si(Li) detectors and two 100-μm thick surface-barrier detectors were exposed to fast neutrons from a calibrated plutonium-beryllium source with detectors reverse biased at the normal operating voltage [400 V for Si(Li) and 30 V for surface-barrier]. Each of the Si(Li) detectors was irradiated to a different fluence, 1×10^9, 5×10^9, or 9.6×10^9 cm^{-2}. All three detectors showed initial increases in leakage current and electronic noise after the bombardment. After the detectors were

annealed at room temperature for about 2 h with bias maintained at 400 V, the current and noise returned to their pre-irradiation values. No change in charge collection efficiency was observed in any of the detectors after the bombardment. Continuous observation over a period of ten weeks showed no further degradation of charge collection efficiency such as had been observed previously in the detectors exposed to higher neutron fluences. The surface-barrier detectors were irradiated with fast neutrons in the range 10^9 to 10^{11} cm^{-2}. No changes in detector characteristics were observed throughout the irradiation. These results, although based on a small sample, seem to indicate that Si(Li) detectors can tolerate up to approximately 10^{10} cm^{-2} fast neutrons while surface-barrier detectors are more radiation resistant and can tolerate fast neutron fluences up to at least 10^{11} cm^{-2}. (Y. M. Liu)

Ambient Exposure Tests — It was determined that the anomalous effect of an increase in current at low pressures, previously reported (NBS Tech. Note 717, p. 41), was due to a defect in the silicon surface-barrier detectors being tested. When different detectors were obtained and tested, no further such problems were encountered.

Measurements of the effects of dry ammonia gas were carried out on three more silicon surface-barrier detectors at pressures from about 0.01 mTorr to 10 Torr. Exposure time varied from 15 to 23 h. No significant changes in either leakage current or noise were observed, in accord with previous results (NBS Tech. Note 702, pp. 33-34). Measurements were also performed on one detector at low pressures of wet ammonia produced by a saturated ammonium hydroxide solution introduced through a variable microleak valve. At pressures from about 0.01 mTorr to 1000 mTorr, no significant changes in either leakage current (0.26 to 0.28 μA) or noise (12.1 to 12.6 keV) were observed. However, some corrosion at the face of the leak valve was detected. The possibility therefore exists that no wet ammonia reached the detector because of the chemical reaction with the leak valve. Wet ammonia was expected to degrade detector characteristics.

Measurements were also carried out at atmospheric pressure using both dry and wet ammonia. Two sources of wet ammonia were used: (1) an open container of ammonium hydroxide placed in the chamber through which dry nitrogen gas was flowed (denoted "NH_4OH"), and (2) an open container of water placed in the chamber through which dry ammonia was flowed (denoted "wet NH_3"). In the atmospheric pressure tests, exposure to dry ammonia for up to 72 h did not affect detector characteristics, whereas exposure to sources of wet ammonia lead to severe degradation in a short time. For example, one detector that had initial current and noise levels of 0.20 μA and 11.2 keV, respectively, showed levels of 0.26 μA and 84.3 keV after 8 min exposure to wet NH_3. Another detector did not appear to be affected by wet NH_3 although exposure to wet nitrogen at atmospheric pressure caused a reversible increase in noise from 13.3 to 20.0 keV.

Table 5 — Summary of Results of Ambient Exposure Tests

Environment	Pressure	Devices	Results
Dry Ammonia	Low	3 Surface-barrier detectors	Did not degrade
	Atmospheric	2 Surface-barrier detectors	Did not degrade
		1 Lithium-drifted slab	Degraded[b]
Dry Hydrogen	Low	2 Surface-barrier detectors	Did not degrade
Methanol	Low	1 Surface-barrier detector	Did not degrade
Wet NH_3	Atmospheric	1 Surface-barrier detector	Did not degrade
		1 Surface-barrier detector	Degraded
NH_4OH	Low[a]	1 Surface-barrier detector	Did not degrade
		1 Germanium mesa diode	Did not degrade[b]
	Atmospheric	2 Surface-barrier detectors	Degraded
		1 Germanium mesa diode	Degraded[b]
Wet Nitrogen	Atmospheric	1 Surface-barrier detector	Degraded

[a] Corrosion at face of leak valve observed (see text)

[b] Unprotected junction

Two detectors were exposed to dry hydrogen gas at pressures ranging from 0.01 to 500 mTorr. No significant changes in either noise or leakage current were observed for exposure times up to 6.5 h.

A summary of the ambient exposure tests and results is given in table 5. In contrast to the sealed commercial devices the lithium-drifted slab detector, fabricated at this laboratory, and the germanium mesa-diode had exposed junctions. These two devices were included in the study in order to aid in the interpretation of the results on the surface-barrier detectors. It can be concluded from the results shown in table 5 that low pressures of dry ammonia or dry hydrogen gas as would obtain in space applications do not affect the performance of commercial silicon surface-barrier detectors in which the junctions are protected. Dry ammonia even at atmospheric pressure appears to have no effect on these devices, although unprotected junctions are subject to degradation. The atmospheric exposure tests would seem to indicate that long-term exposure to dry ammonia at low pressures will not seriously degrade detector performance. The variability in detector response to the corrosive wet ammonia at atomspheric pressure (one device did not degrade after 4 h, while a second suffered degradation after only 8 min) may also be explained on the basis of the integrity of the detector mount.

(W. K. Croll)

Plans: The results of the studies of electron, proton, and neutron radiation damage effects in lithium-drifted silicon detectors will be prepared for publication. No further work on exposure of detectors to potentially harmful ambients is contemplated following a final report of results to the sponsor.

5.5. REFERENCES

5.1. Thermal Properties of Devices

1. Oettinger, F. F., and Rubin, S., The Use of Current Gain as an Indicator for the Formation of Hot Spots Due to Current Crowding in Power Transistors, presented at the 1972 IEEE Reliability Physics Symposium, Las Vegas, Nevada, April 5, 1972.

5.3. Carrier Transport in Junction Devices

1. Smith, K. R., Scattering Parameter Method of Determining Base Transit Time for Bipolar Transistors, Report No. RL-TM-70-2, USAMC, Redstone Arsenal, April, 1970. Available to qualified users from the Defense Documentation Center, Cameron Station, Alexandria, Virginia 22314, Accession Number AD 875684.

APPENDIX A
JOINT PROGRAM STAFF

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APPENDIX B
COMMITTEE ACTIVITIES

ASTM Committee F-1 on Electronics

C. F. Bolton, Committee Assistant Secretary

W. M. Bullis, Editor, Subcommittee 4, Semiconductor Crystals, and Subcommittee 7, Hybrid Microelectronics; Leaks, Resistivity, Mobility, Dielectrics, and Compound Semiconductors Sections

J. R. Ehrstein, Chairman, Resistivity Section; Epitaxial Resistivity, and Epitaxial Thickness Sections

J. C. French, Committee Editor

G. G. Harman, Interconnection Bonding Section

K. O. Leedy, Chairman, Interconnection Bonding Section

T. F. Leedy, Photoresist Section

C. P. Marsden, Committee Secretary

R. L. Mattis, Lifetime Section

W. E. Phillips, Chairman, Lifetime Section; Secretary, Subcommittee 4, Semiconductor Crystals; Crystal Perfection, Encapsulation, Thin Films, and Thick Films Section

A. H. Sher, Germanium Section

W. R. Thurber, Mobility, Germanium, Compound Semiconductors, and Impurities in Semiconductors Sections

ASTM Committee E-10 on Radioisotopes and Radiation Effects

W. M. Bullis, Subcommittee 7, Radiation Effects on Electronic Materials

J. C. French, Subcommittee 7, Radiation Effects on Electronic Materials

Electronic Industries Association: Solid State Products Division, Joint Electron Device Engineering Council (JEDEC)

J. M. Kenney, Microwave Diode Measurements, Committee JC-21 on UHF and Microwave Diodes

F. F. Oettinger, Chairman, Task Group JC-11.3-1 on Thermal Considerations for Microelectronic Devices, Committee JC-11 on Mechanical Standardization; Technical Advisor, Thermal Resistance Measurements, Committees JC-22 on Rectifier Diodes and Thyristors, JC-20 on Signal Diodes, JC-25 on Power Transistors, and JC-30 on Hybrid Integrated Circuits

S. Rubin, Chairman, Council Task Group on Galvanomagnetic Devices

H. A. Schafft, Technical Advisor, Second Breakdown and Related Specifications, Committee JC-25 on Power Transistors

IEEE Electron Devices Group:

J. C. French, Standards Committee

J. M. Kenney, Chairman, Standards Committee Task Force on Microwave Solid-State Devices II (Mixer and Video Detector Diodes)

H. A. Schafft, Chairman, Standards Committee Task Force on Second Breakdown Measurement Standards

IEEE Magnetics Group

S. Rubin, Chairman, Galvanomagnetic Standards Subcommittee

IEEE Parts, Hybrids, and Packaging Group

W. M. Bullis, New Technology Subcommittee, Technical Committee on Hybrid Microelectronics

Society of Automotive Engineers

J. C. French, Subcommittee A-2N on Radiation Hardness and Nuclear Survivability

W. M. Bullis, Planning Subcommittee of Committee H on Electronic Materials and Processes

IEC TC47, Semiconductor Devices and Integrated Circuits:

S. Rubin, Technical Expert, Galvanomagnetic Devices; U.S. Specialist for Working Group 5 on Hall Devices and Magnetroresistive Devices

NMAB ad hoc Committee on Materials and Processes for Electron Devices

W. M. Bullis

NMAB ad hoc Committee on Materials for Radiation Detection Devices

D. E. Sawyer

APPENDIX C
SOLID-STATE TECHNOLOGY & FABRICATION SERVICES

Technical services in areas of competence are provided to other NBS activities and other government agencies as they are requested. Usually these are short-term, specialized services that cannot be obtained through normal commercial channels. Such services provided during the last quarter are listed below and indicate the kinds of technology available to the program.

1. Failure Analysis (W. J. Keery)

Material from an aircraft air conditioning unit was inspected by means of scanning electron microscopy and x-ray energy analysis for the presence of foreign particles for the Naval Weapons Engineering Support Activity.

2. Thermal Converter (H. K. Kessler)

A thin-film multijunction thermal converter was repaired for the Electrical Instruments Section.

3. Photosensitive Diodes (T. F. Leedy)

Photosensitive diodes with an effective junction area of about 0.25 mm^2 were fabricated by alloying gold into gadolinium-doped germanium cubes measuring 0.87 mm on a side for the Harry Diamond Laboratories.

APPENDIX D
JOINT PROGRAM PUBLICATIONS

Prior Reports:

A review of the early work leading to this Program is given in Bullis, W. M., Measurement Methods for the Semiconductor Device Industry — A Review of NBS Activity, NBS Tech. Note 511, December, 1969.

Quarterly reports covering the period since July 1, 1968, have been issued under the title Methods of Measurement for Semiconductor Materials, Process Control, and Devices. These reports may be obtained from the Superintendent of Documents (Catalog Number C.13.46:XXX) where XXX is the appropriate technical note number. Microfiche copies are available from the National Technical Information Service (NTIS), Springfield, Virginia 22151.

Quarter Ending	NBS Tech. Note	Date Issued	NTIS Accession No.
September 30, 1968	472	December, 1968	AD 681330
December 31, 1968	475	February, 1969	AD 683808
March 31, 1969	488	July, 1969	AD 692232
June 30, 1969	495	September, 1969	AD 695820
September 30, 1969	520	March, 1970	AD 702883
December 31, 1969	527	May, 1970	AD 710906
March 31, 1970	555	September, 1970	AD 718534
June 30, 1970	560	November, 1970	AD 719976
September 30, 1970	571	April, 1971	AD 723671
December 31, 1970	592	August, 1971	AD 728611
March 31, 1971	598	October, 1971	AD 732553
June 30, 1971	702	November, 1971	AD 734427
September 30, 1971	717	April, 1972	

Current Publications:

As various phases of the work are completed, publications are prepared to summarize the results or to describe the work in greater detail. Copies of most of such publications are available and can be obtained on request to the editor or the author.

Sher, A. H., and Thurber, W. R., Minority Carrier and Lithium-Ion Drift Mobilities and Oxygen Concentration in *p*-Type Germanium, *J. Appl. Phys.* 42, 4508-4509 (October, 1971).

Sher, A. H., Croll, W. K., and Thurber, W. R., Determination of Oxygen in Germanium Below 20 Parts per Billion by Measurements of Lithium Mobility and Precipitation, *Anal. Chem.* 43, 1831-1834 (November, 1971).

Sher, A. H., Keery, W. J., and Dyson, H. E., Improved Infrared Response Measurements in Semiconductor Nuclear Radiation Detectors, presented at the 1971 Nuclear Science Symposium, San Francisco, November 5, 1971, *IEEE Trans. Nucl. Sci.* NS-19, No. 1, 341-344 (February, 1972).

Schafft, H. A., Wire-Bond Electrical Connections: Testing, Fabrication and Degradation, A Bibliography — 1957-1971, Technical Note 593 (January, 1972).

Sher, A. H., and Keery, W. J., Improved Infrared-Response Technique for Determining Impurity and Defect Levels in Semiconductors, *Appl. Phys. Lett.* 20, 120-122 (1 February 1972).

Marsden, C. P., Tabulation of Data on Semiconductor Amplifiers and Oscillators at Microwave Frequencies, NBS Technical Note 597 (December, 1971). (Supersedes NBS Technical Note 518).

Marsden, C. P., Tabulation of Published Data on Electron Devices of the U.S.S.R. Through December 1971, NBS Technical Note 715 (February, 1972). (Supersedes NBS Technical Note 526).

Thurber, W. R., and Bullis, W. M., Resistivity and Carrier Lifetime in Gold-Doped Silicon, AFCRL Report AFCRL-72-0076, January 31, 1972.

Phillips, W. E., Interpretation of Steady-State Surface Photovoltage Measurements in Epitaxial Semiconductor Layers, to be published in *Solid-State Electronics*.

Sher, A. H., Liu, Y. M., and Keery, W. K., Infra-Red Response Measurements on Radiation-Damaged Si(Li) Detectors, presented at the 13th Scintillation and Semiconductor Counter Symposium, Washington, D. C., March 3, 1972, to be published in *IEEE Trans. Nucl. Sci.* (June, 1972).

Liu, Y. M., and Coleman, J. A., Radiation Damage Effects by Electrons, Protons and Neutrons in Si(Li) Detectors to be published in *IEEE Trans. Nucl. Sci.* (June, 1972).

Harman, G. G., and Leedy, K. O., An Experimental Model of the Microelectronic Ultrasonic Wire Bonding Mechanism, presented at the 1972 Reliability Physics Symposium, Las Vegas, Nevada, April 5, 1972.

Oettinger, F. F., and Rubin, S., The Use of Current Gain as an Indicator for the Formation of Hot Spots Due to Current Crowding in Power Transistors, presented at 1972 Reliability Physics Symposium, Las Vegas, Nevada, April 5, 1972.

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7. AUTHOR(S)

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16. ABSTRACT (A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.)

This quarterly progress report, fourteenth of a series, describes NBS activities directed toward the development of methods of measurement for semiconductor materials, process control, and devices. Significant accomplishments during this reporting period include the determination of the reasons for substantial differences in measurements of transistor delay time, a device characteristic frequently used as a screen in radiation hardness assurance tests, as measured with different instruments or with the same instrument at different frequencies; identification of an energy level model for gold-doped silicon that yields a calculated dependence of resistivity on gold concentration that agrees very well with experimental measurements on *p*-type gold-doped silicon; and finding of evidence that it does not appear to be necessary for an ultrasonic bonding tool to grip the wire and move it across the substrate metallization to make the bond. Work is continuing on measurement of resistivity of semiconductor crystals; study of gold-doped silicon; development of the infrared response technique; evaluation of wire bonds and die attachment; measurement of thermal properties of semiconductor devices, delay time and related carrier transport properties in junction devices, and noise properties of microwave diodes; and characterization of silicon nuclear radiation detectors. Supplementary data concerning staff, standards committee activities, technical services, and publications are included as appendixes.

Key Words (cont.): measurement; microelectronics; microwave diodes; nuclear radiation detectors; probe techniques (a-c); resistivity; semiconductor devices; semiconductor materials; semiconductor process control; silicon; thermal resistance; thermographic measurements; ultrasonic bonding; wire bonds.

17. KEY WORDS (Alphabetical order, separated by semicolons) Alpha-particle detectors; aluminum wire; base transit time; carrier lifetime; die attachment; electrical properties; epitaxial silicon; gamma-ray detectors; germanium; gold-doped silicon; infrared response; methods of

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215